P67xx Series
Serial Analyzer Probes Design Guide &
Instruction Manual

www.tektronix.com
071-2088-02

Tektronix

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of a larger system. Read the safety sections of the other component manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Connect and Disconnect Properly. Connect the probe output to the measurement instrument before connecting the probe to the circuit under test. Connect the probe reference lead to the circuit under test before connecting the probe input. Disconnect the probe input and the probe reference lead from the circuit under test before disconnecting the probe from the measurement instrument.

Ground the Product. This product is indirectly grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

The inputs are not rated for connection to mains or Category II, III, or IV circuits.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Power Disconnect. The power cord disconnects the product from the power source. Do not block the power cord; it must remain accessible to the user at all times.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Do Not Operate With Suspected Failures. If you suspect that there is damage to this product, have it inspected by qualified service personnel.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Terms in this Manual

These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Symbols and Terms on the Product

These terms may appear on the product:

- DANGER indicates an injury hazard immediately accessible as you read the marking.
- WARNING indicates an injury hazard not immediately accessible as you read the marking.
- CAUTION indicates a hazard to property including the product.

The following symbol(s) may appear on the product:

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, switch off the instrument power, then disconnect the power cord from the mains power.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Environmental Considerations

This section provides information about the environmental impact of the product.

Product End-of-Life Handling

Observe the following guidelines when recycling an instrument or component:

Equipment Recycling. Production of this equipment required the extraction and use of natural resources. The equipment may contain substances that could be harmful to the environment or human health if improperly handled at the product's end of life. In order to avoid release of such substances into the environment and to reduce the use of natural resources, we encourage you to recycle this product in an appropriate system that will ensure that most of the materials are reused or recycled appropriately.

This symbol indicates that this product complies with the European Union's requirements according to Directive 2002/96/EC on waste electrical and electronic equipment (WEEE). For information about recycling options, check the Support/Service section of the Tektronix Web site (www.tektronix.com).

Restriction of Hazardous Substances

This product has been classified as Monitoring and Control equipment, and is outside the scope of the 2002/95/EC RoHS Directive. This product complies with the RoHS Directive requirements except for the presence of hexavalent chromium in the surface coating of the aluminum chassis parts, assembly hardware, and 63/37 tin/lead solder used in the fabrication of the circuit boards.

Preface

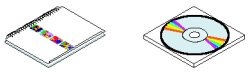
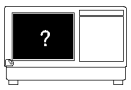
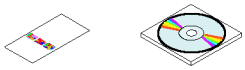
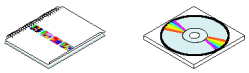
This manual contains information needed to install and use a P67xx Series probe with a TLA7S08 or TLA7S16 Serial Analyzer module to debug, validate, and verify computer and embedded systems.

Related Documentation

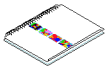
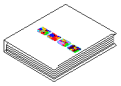
The following table lists related documentation available for your instrument. The documentation is available on the TLA Documentation CD and on the Tektronix Web site (www.Tektronix.com/manuals).

For documentation not specified in the table, contact your local Tektronix representative.

Related Documentation

Item	Purpose	Location
TLA Quick Start User Manuals	High-level operational overview	
Online Help	In-depth operation and UI help	
Installation Quick Reference Cards	High-level installation information	
Installation Manuals	Detailed first-time installation information	
XYZs of Logic Analyzers	Logic analyzer basics	 www.Tektronix.com
Decalcification and Securities instructions	Data security concerns specific to sanitizing or removing memory devices from Tektronix products	 www.Tektronix.com
Application notes	Collection of logic analyzer application specific notes	
Product Specifications & Performance Verification Procedures	TLA Product specifications and performance verification procedures	
TPI.NET Documentation	Detailed information for controlling the logic analyzer using .NET	

Related Documentation (cont.)

Item	Purpose	Location
Field upgrade kits	Upgrade information for your logic analyzer	 
Optional Service Manuals	Self-service documentation for modules and mainframes	 

List of Terms

The following is a list of terms that appear in this manual. You may want to review this list if you are unfamiliar with some of the terms. For a list of PCI Express®-specific terms, refer to the PCI Express Base Specification.

Table i: Terms used in this document

Term	Description
Footprint	An arrangement of pads built into the board as specified in the PCI Express Base Specification. It is the contact point for the retention mechanism.
Retention Mechanism	The mechanism that connects the probe head to the PCB. It fits on the footprint and must be soldered to the PCB.
Probe Head	The end of the probe that connects to the retention mechanism.
Full-width	16-Channel
Half-width	8-Channel
Link	A connection between two PCI Express devices. A link consists of a number of lanes. A link described as by-N (or xN) consists of a number (N) lanes.
Differential Pair	A set of two signals, positive and negative, transmitting data from one device to another.
Lane	A single differential pair (two signals) that transmit data in one direction of a PCI Express Link. A unidirectional lane.
PCB	Printed circuit board
SUT	System under test. This is the system/circuit board(s) you intend to test with the serial analyzer.

Getting Started

Product Description

Tektronix offers three types of probes for the TLA7S08 and TLA7S16 Serial Analyzer modules:

- Mid-bus probes
- Slot interposer probes
- Solder-down probes

Mid-Bus Probes

A mid-bus probe connects to a retention mechanism installed on your circuit board. You must install the retention mechanism to either a PCI Express Gen1 or Gen2 footprint on your circuit board.

Tektronix offers the following mid-bus probes:

- P6708 8-Channel Mid-bus probe
- P6716 16-Channel Mid-bus probe

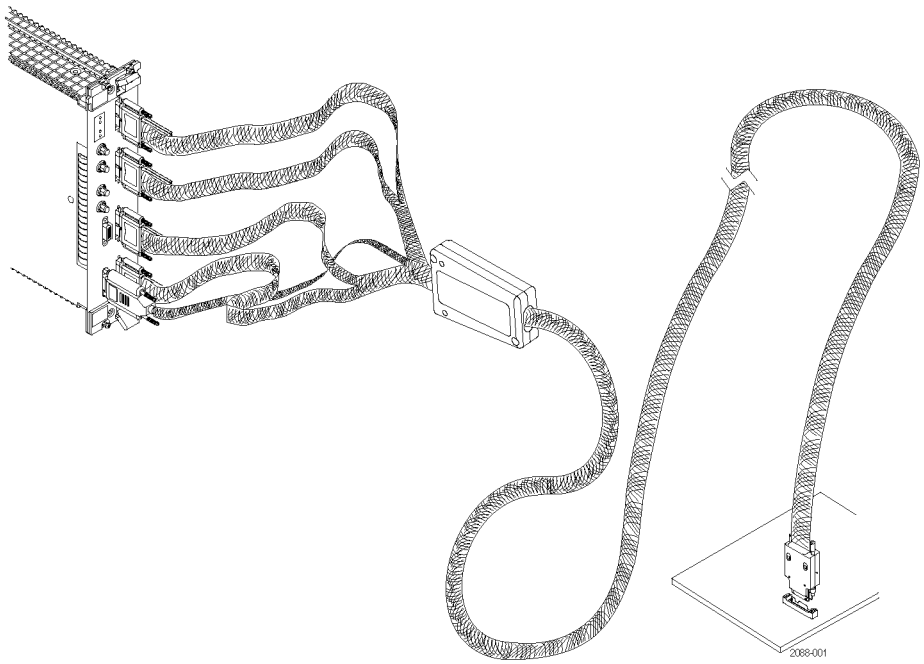


Figure 1: P6716 16-Channel mid-bus probe

Slot Interposer Probes

A slot interposer probe connects to a PCI Express slot on your SUT. Each probe has a x16 connector for a PCI Express card device.

Tektronix offers the following (bidirectional) slot interposer probes:

- P6701SP PCI Express x1 Slot Interposer probe
- P6704SP PCI Express x4 Slot Interposer probe
- P6708SP PCI Express x8 Slot Interposer probe
- P6716SP PCI Express x16 Slot Interposer probe

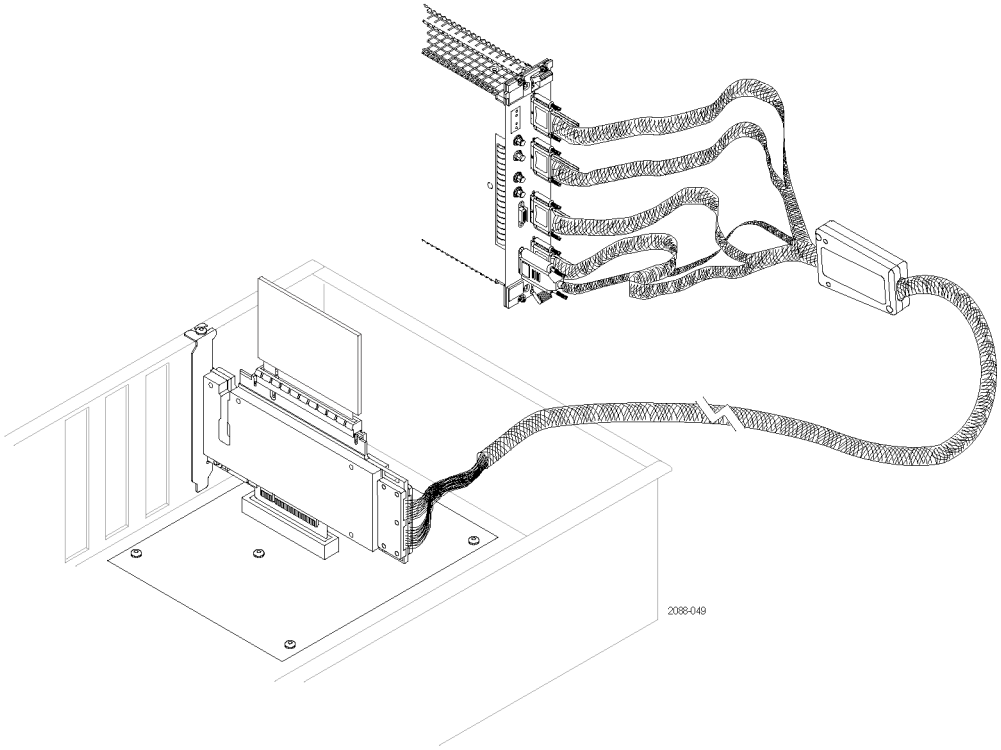


Figure 2: P6708SP Slot interposer probe

P6701SD Solder-Down Probe

The P6701SD probe connects to your SUT through the differential solder-down tip (P75TLRST). Up to four probes (one differential pair each) can be installed in each signal connector to the serial module. (See page 57, *Adding Probes to the P6701SD Probe Connector*.)

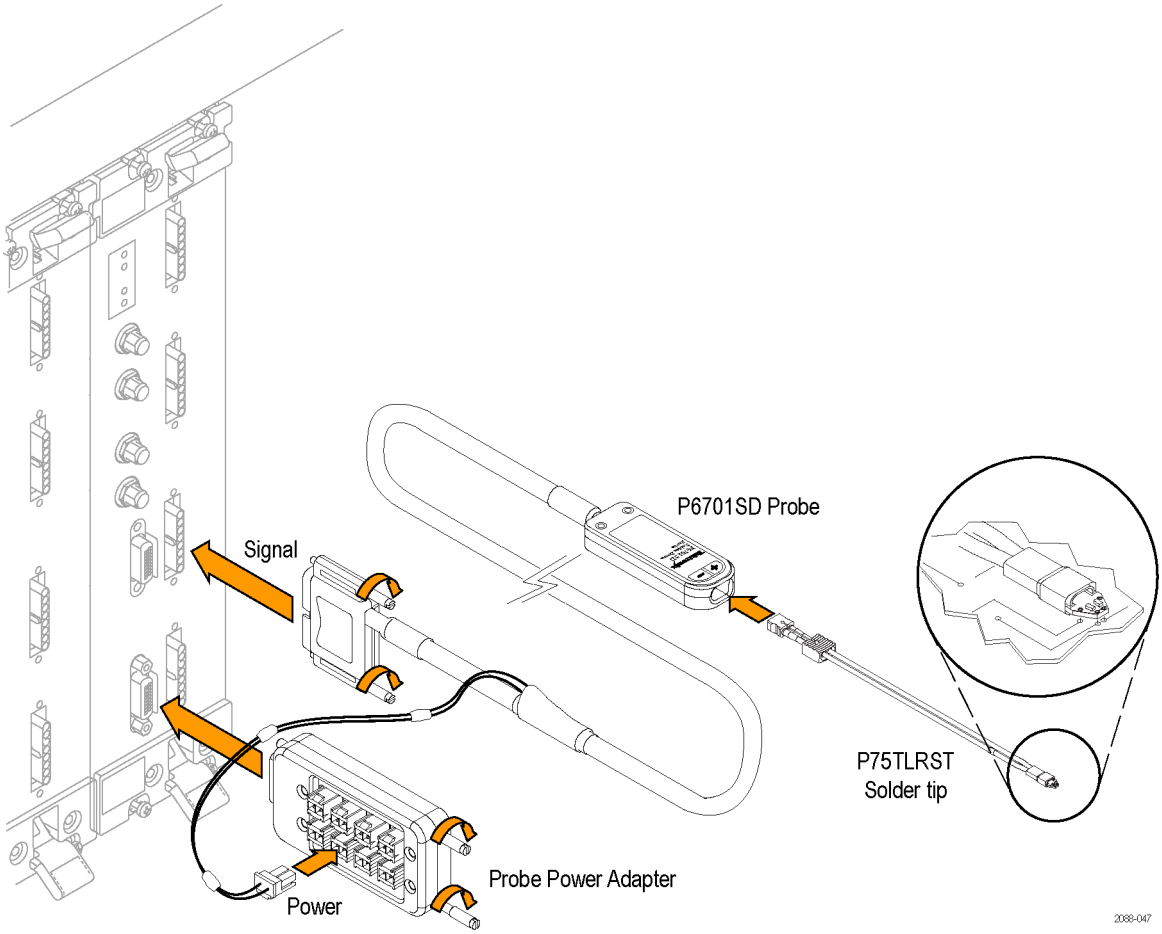


Figure 3: P6701SD Solder-Down probe

Operating Basics

Preparing for Installation of the Mid-bus Retention Mechanism

Cleaning the Footprint

Inspect the footprint for lint, oil, or fingerprints. If the footprint is dirty, clean it by following these steps:

CAUTION. *To avoid electrical damage, always power off your system under test before cleaning the footprint.*

1. Use a lint-free, clean-room cloth lightly moistened with electronic/reagent grade isopropyl alcohol, and gently wipe the surface of the footprint.
2. Remove any remaining lint using a nitrogen air gun or clean, oil-free dry air.

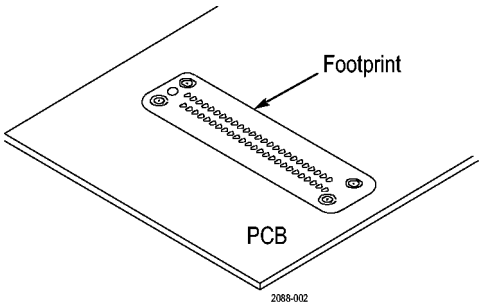


Figure 4: 16-Channel footprint

Installing the Mid-bus Retention Mechanism

Before connecting a mid-bus probe, you must install the retention mechanism. The retention mechanism connects the probe head to your circuit board (PCB). It fits on the footprint and must be soldered to the PCB. To install the retention mechanism on the circuit board, do the following:

1. Locate the correct footprint. If you intend to use multiple probes, your PCB has multiple footprints. Be careful to select the correct one.
2. Align the retention mechanism over the footprint so that the keying pin on the retention mechanism lines up with the keying pin hole on the footprint. (See Figure 5.)
3. Insert the retention mechanism into the holes in the footprint on the PCB.

NOTE. *The following two steps are important to ensure that the retention mechanism is correctly mounted and that the probe makes proper contact with the PCB.*

4. Hold the retention mechanism so that it is firmly flush with the surface of the footprint, and the four anchoring posts extend through the circuit board to the opposite side.

5. Using a pair of needle-nose pliers, grasp one of the posts. Using the circuit board hole as a fulcrum, bend the post outward so that it secures the mechanism to the PCB. Bend the other three posts in the same manner.

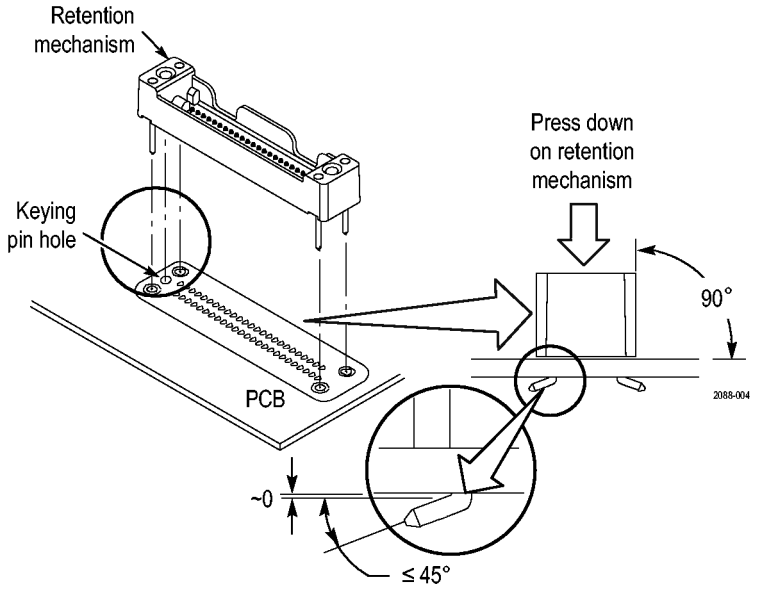


Figure 5: Installing the retention mechanism

6. Solder the anchoring posts to the PCB.

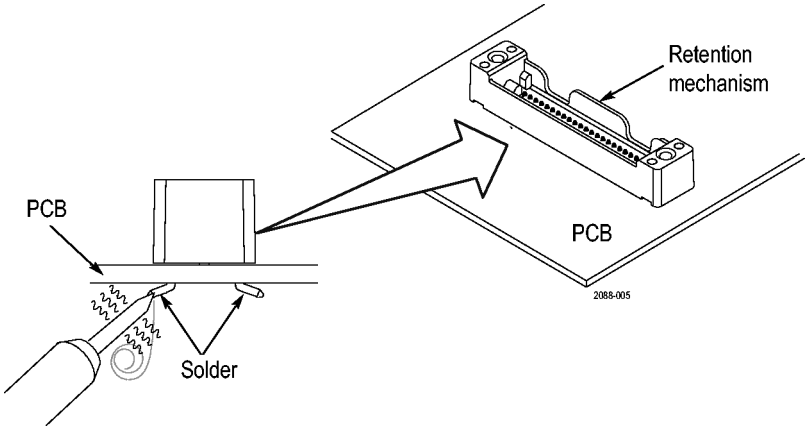


Figure 6: Soldering the anchoring posts to the PCB

Connecting the Mid-bus Probe

After you have installed the retention mechanism, you are ready to connect the mid-bus probe.

Handling the Probe Head

Handle the probe head with care. Keep the following points in mind:

- Handle the probe head by the outer plastic casing. Do not touch the contacts in the center with fingers, tools, wipes, or any other devices.
- Do not expose the connector to liquids or dry chemicals.
- When connecting the probe, be careful not to touch the probe head contacts to any other surfaces or components on your circuit board.

Connect the Probe

Connect the probe by following these steps:

1. Locate the correct retention mechanism. If you intend to use multiple probes, your PCB has multiple retention mechanisms. Be careful to select the correct one.
2. Align the probe head with the retention mechanism. Both are keyed so that the probe can only be inserted one way.
3. Press the probe head into the retention mechanism.

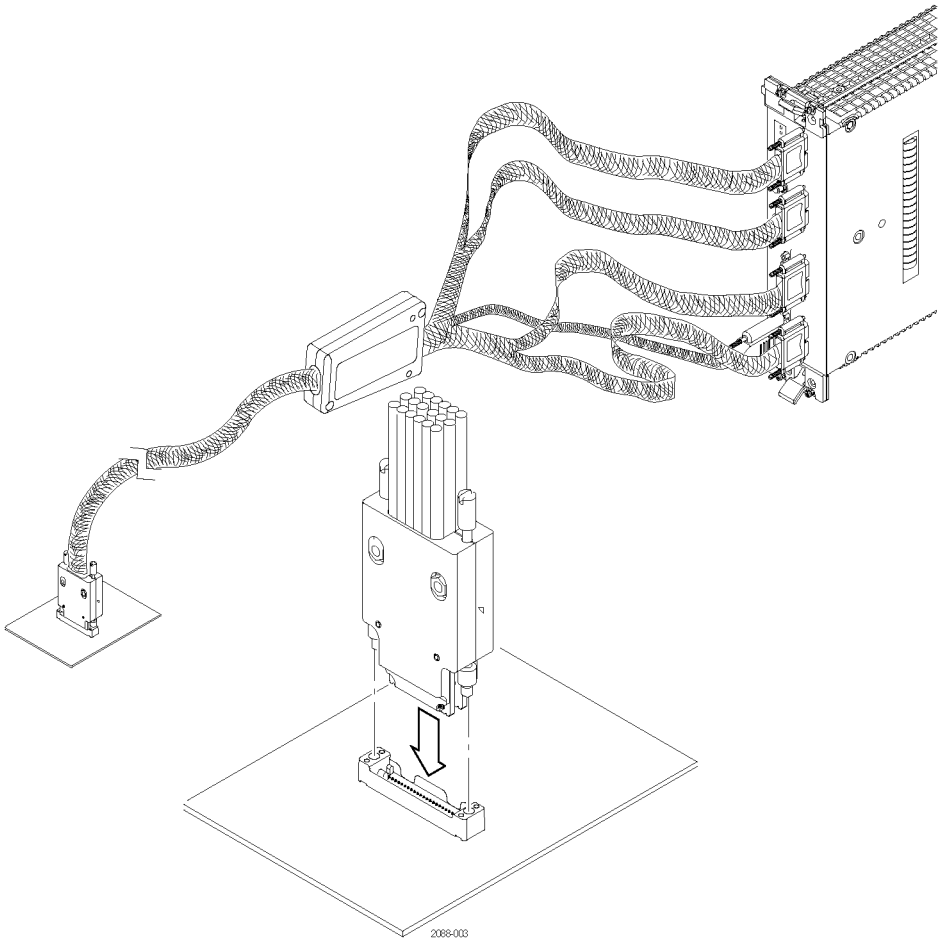


Figure 7: Connecting a probe to the retention mechanism

4. Start both mounting screws in the posts, and tighten them evenly to ensure that the probe approaches and mates squarely to the PCB. If access is limited, use the adjustment tool included with your probe. The probe is completely fastened to the PCB when both mounting screws are seated.

5. Refer to the *TLA7S08 & TLA7S16 Serial Analyzer Modules Instruction Manual* to verify that all channels are acquiring data. If you suspect that a poor probe connection may be the source of a problem, refer to the troubleshooting section of the *TLA7S08 & TLA7S16 Serial Analyzer Modules Instruction Manual*.

Arranging the Mid-bus Probe Cables

Arrange and hang the probe cables so that the probe head is perpendicular to the circuit board, and tension on the retention mechanism is minimized. Route the cables as straight as possible, maximizing the bend radius, and make sure that a 90 degree bend does not occur within three inches of the circuit board surface. (See Figure 8.) You can route a hanger through the two holes in the cable transition housing as well.

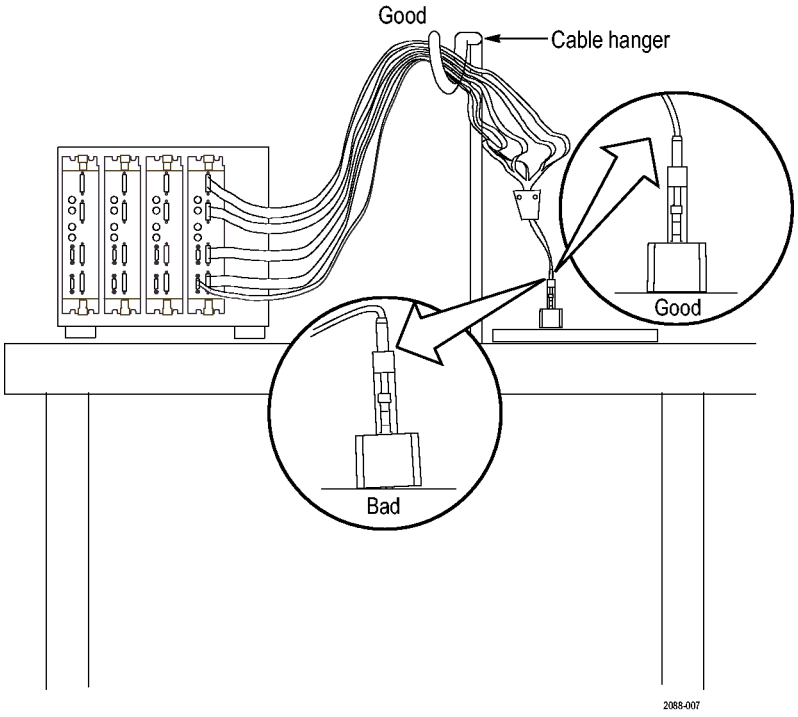


Figure 8: Arranging the mid-bus probe cables

Connecting a Slot Interposer Probe

Handling the Probe Head

Handle the probe head with care. Keep the following points in mind:

- Handle the probe head by the outer casing. Do not touch the contacts with fingers, tools, wipes, or any other devices.
- Do not expose the connector to liquids or dry chemicals.
- When connecting the probe, be careful not to touch the probe head contacts to any other surfaces or components on your circuit board.

CAUTION. *Static discharge can damage the probe head. Always wear a grounded antistatic wrist strap whenever handling the probe head. Also verify that anything to which the probe head is connected does not carry a static charge.*

Connect the Probe

Connect the probe by following these steps:

1. Disconnect the power supply to your SUT. Unplug the PC power supply if your SUT is connected to one.
2. Locate the correct PCI Express slot.
3. Align the probe with the slot.
4. Press the probe head into the slot.

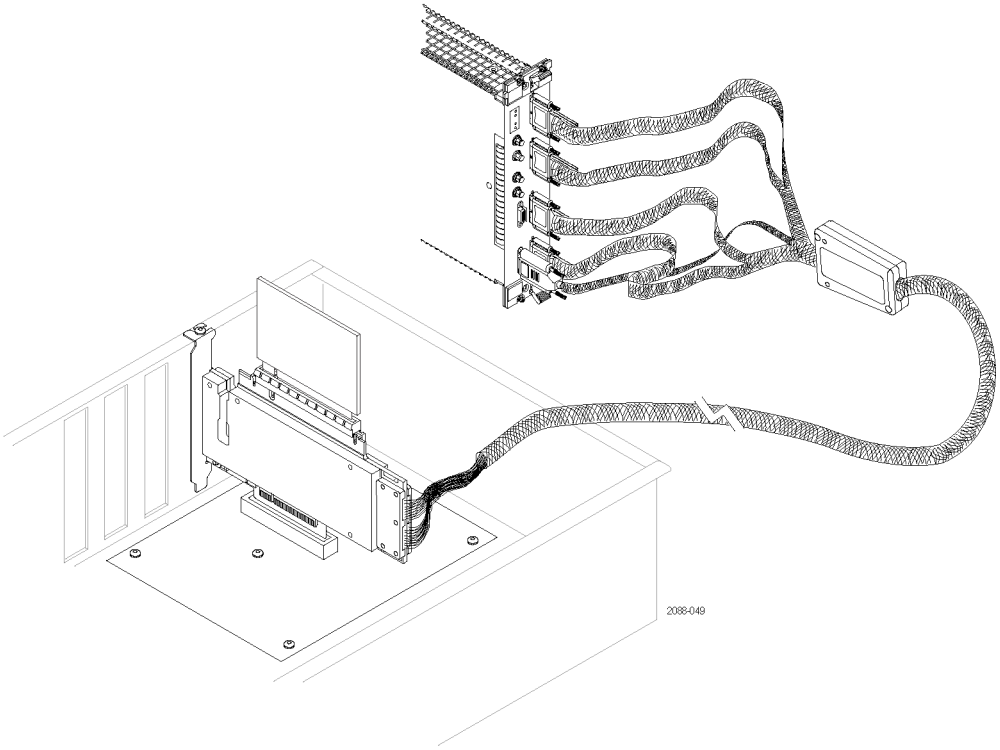


Figure 9: Connecting a slot interposer probe

5. Position the mounting bracket and attach the screws.
6. Press your PCI Express card device into the probe.

NOTE. *When the slot interposer is installed, you must connect the power connector to the module and the module must be powered on whenever the SUT is powered on.*

7. Refer to the *TLA7S08 & TLA7S16 Serial Analyzer Modules Instruction Manual* to verify that all channels are recognizing signals. If you suspect that a poor probe connection may be the source of a problem, refer to the troubleshooting section of the *TLA7S08 & TLA7S16 Serial Analyzer Modules Instruction Manual*.

Connecting the Solder-Down Probe

The probe connects to the module and to the probe tip, and the probe tip is soldered to the circuit. Install the probe by following these steps:

Connect to the Serial Analyzer Module

1. Plug the signal connector into the module and tighten the hold-down screws.
2. Plug the Power Adapter into the module and tighten the hold-down screws.
3. Plug the power connector into any one of the receptacles on the Power Adapter.

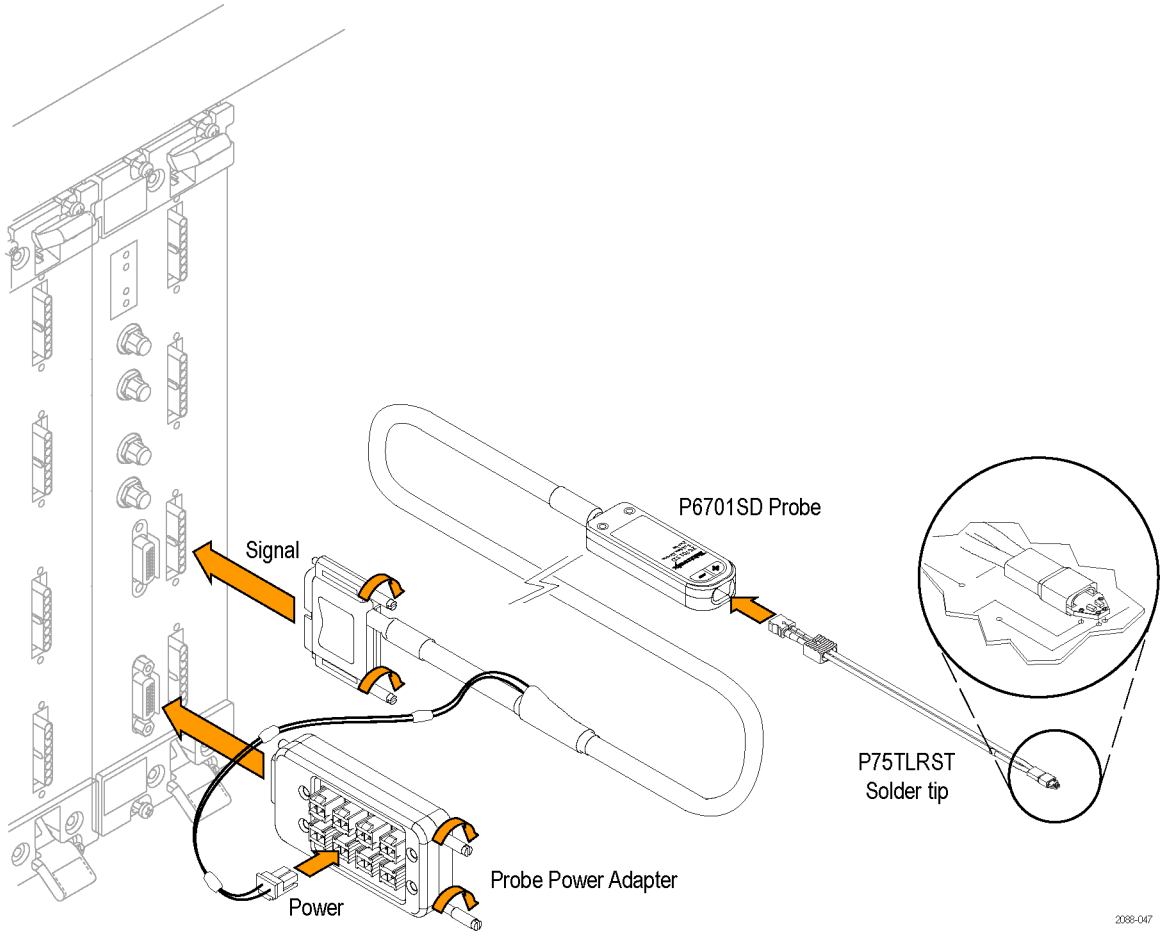


Figure 10: Installing the P6701SD probe

P75TLRST Solder Tip

Install the probe tip by following these steps:

NOTE. *This tip is very small and must be handled carefully. The following procedures describe the proper techniques for using the tip.*

Connect to the Probe Head. The probe body and tip cable ends are keyed to ensure correct installation.

1. Orient the probe body with the + and – inputs on top.
2. Align the tip cable lead with the red band to the + input.

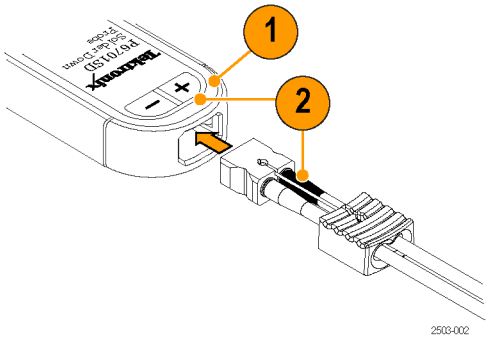


Figure 11: Connecting the P75TLRST tip to the probe head

3. Grasp the cable connector by hand and push the cable into the probe body until you feel a click. The cable housing is fully seated when it is flush with the edge of the probe body.
4. To remove the tip, pull the cable tab straight out from the probe body.

CAUTION. *Pull only on the cable tab when removing the tip. You can damage the tip or probe if you pull on the cables.*

Connect to the Circuit. The dimensions of the solder tip connections are provided in this manual for reference. (See Figure 34 on page 32.) You can also design the tip footprint into your circuit board layout for easier test connections.

To connect the probe tip to your circuit, use the wire and solder that are provided in the wire replacement kit. The kit includes:

- 0.004 in (0.1016 mm) wire
- 0.008 in (0.2032 mm) wire
- SAC305 solder (RoHS compliant)

1. Identify a location where the tip can be placed, soldered, and secured to your circuit. You can work with long wires (~1 inch), but keep the finished wire lengths of the signal and ground connections as short as possible.
2. Lay the wires against a circuit board pad, trace, or other conductive feature. (If vias or through-holes are very close, you can thread the wires through them.)
3. Solder the wires to your circuit.

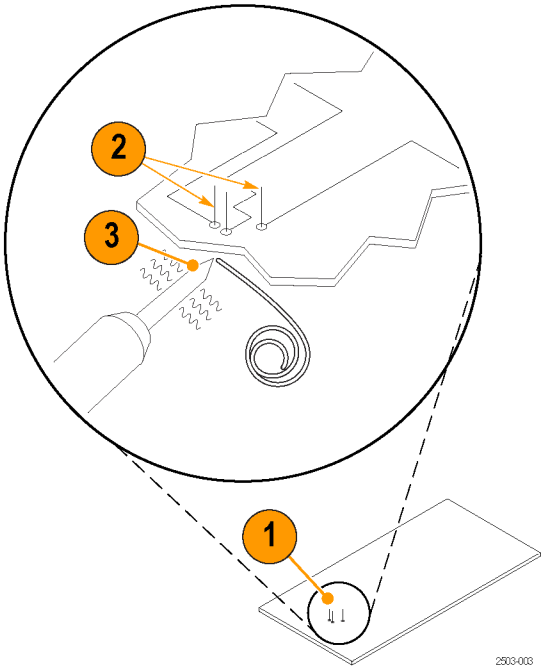


Figure 12: Connecting wires to the circuit

4. Attach tip tape to the bottom of the tip.
5. Clean out the tip vias with a solder-wicking material if you are reusing the tip. Thread the wires through the tip.
6. Press the tip to the circuit board and quickly solder the wires to the tip. Keep all finished wire lengths as short as possible.
7. Clip off the excess wire from all of the solder joints.
8. Push the end of the tip into the probe head until it seats in the probe head.

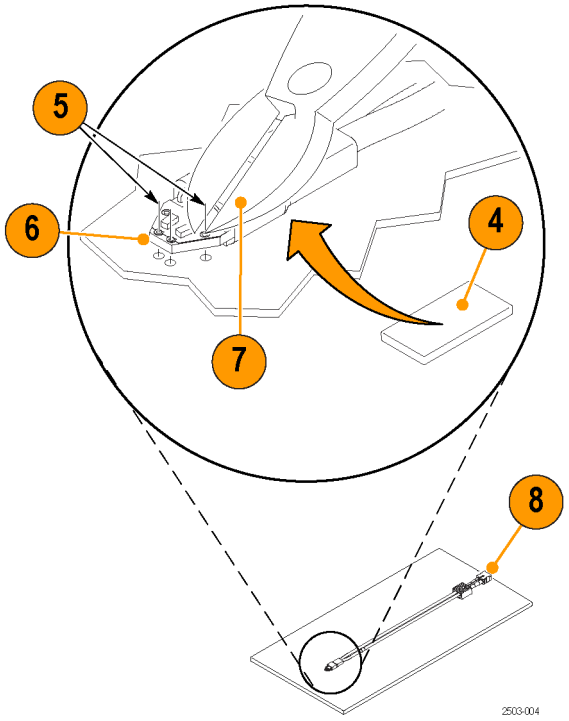


Figure 13: Connecting the tip to the circuit

9. Secure the probe to the circuit board with tape or with the hook-and-loop strips and dots that are included with the probe.

Reference

This section provides guidelines for designing a system to be tested with a P67xx series probe(s).

Probe Dimensions

The following figure shows dimensions of the P67xx series probes. Both the P6708 and P6716 have the same cable lengths.

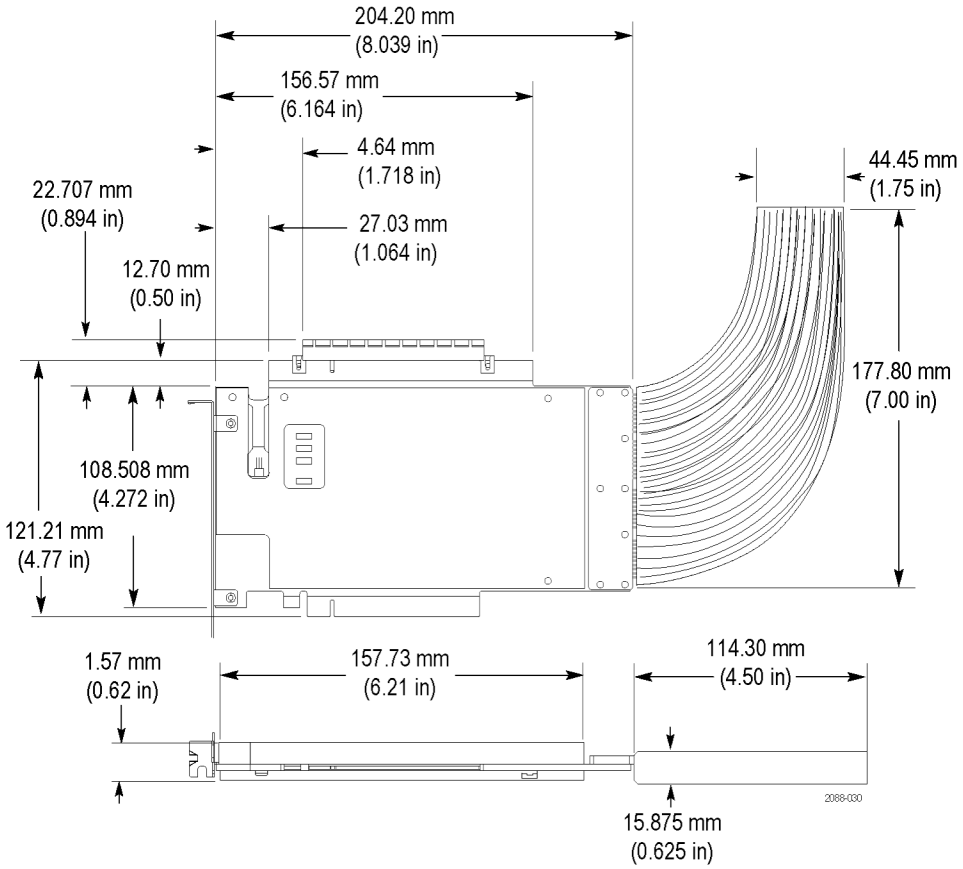


Figure 14: P6716SP dimensions

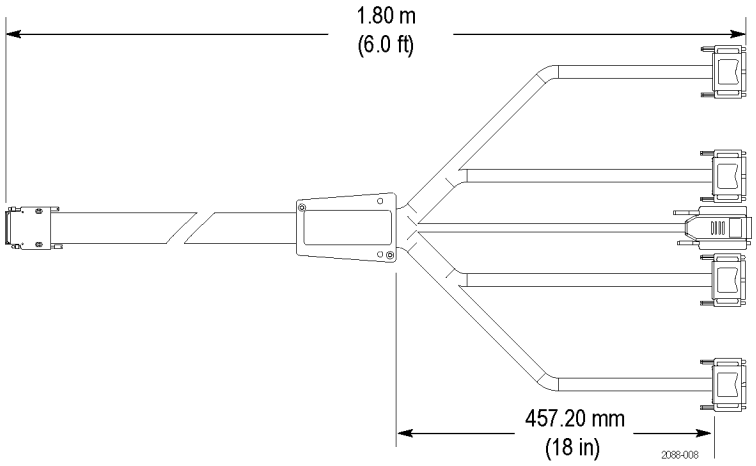


Figure 15: P6716 cable length dimensions

The following figures show the dimensions of the P67xxSP slot interposer probes.

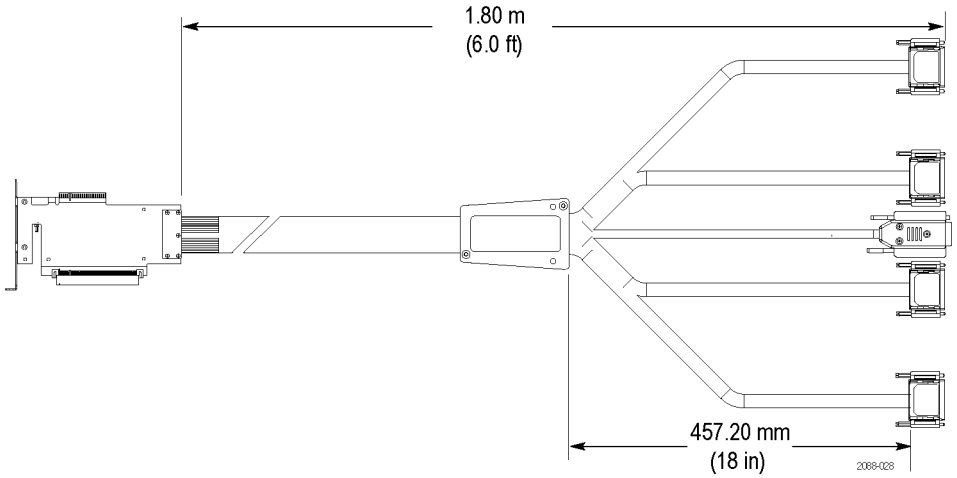


Figure 16: P6716SP cable length dimensions

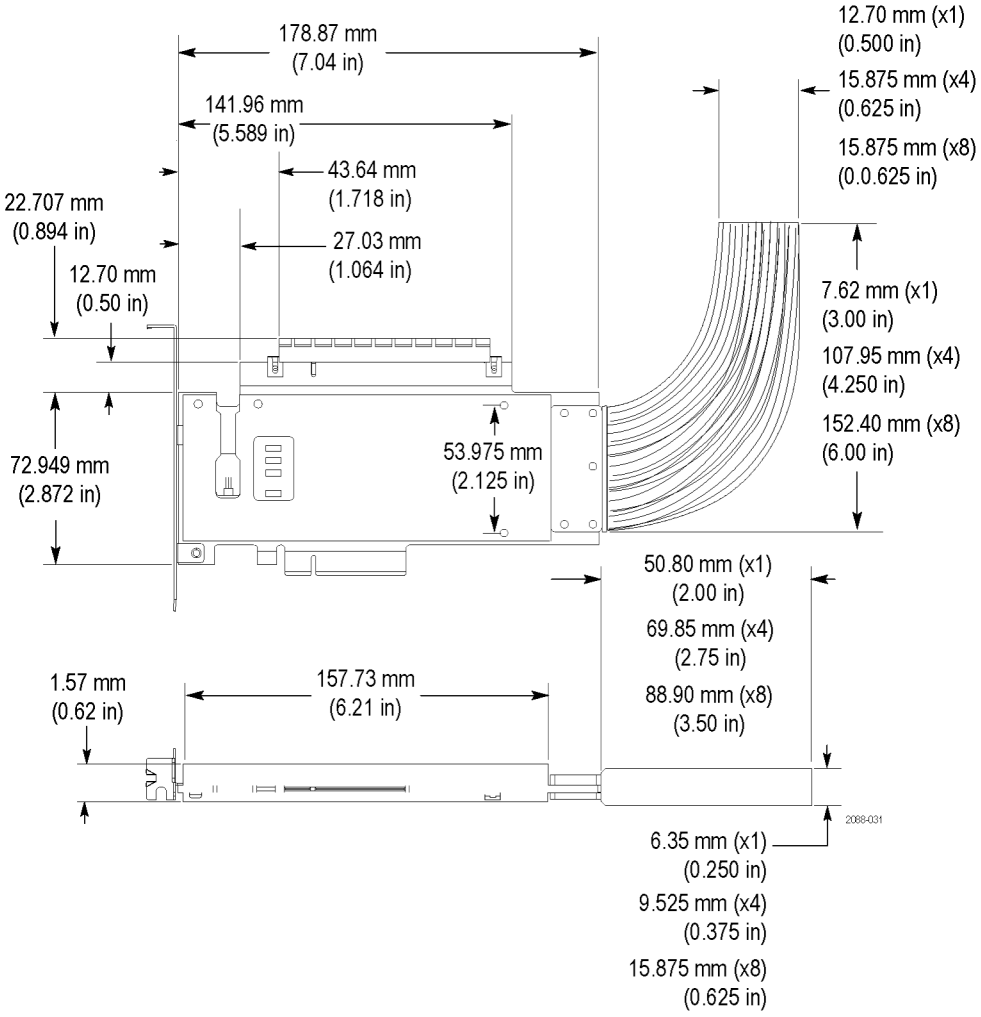


Figure 17: P6701SP, P6704SP, and P6708SP dimensions

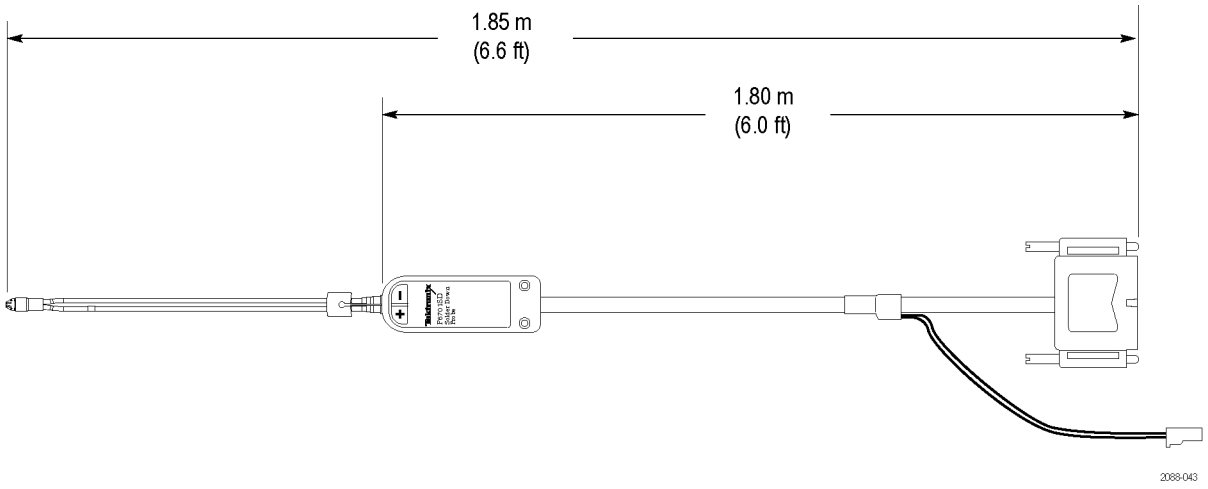


Figure 18: P6701SD dimensions

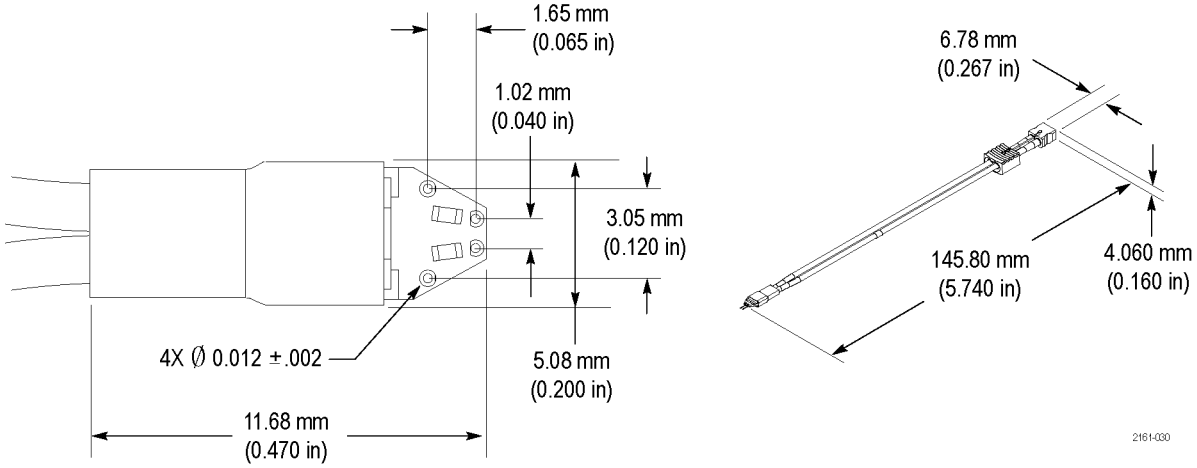


Figure 19: P75TLRST Solder Tip dimensions

Circuit Board Design

Use the following mechanical and electrical guidelines when designing your system.

Mechanical Design

This section provides mechanical design details for the mid-bus probe, including footprint dimensions, footprint keep-out areas, and trace and via size, and routing requirements.

Table 1: Recommended circuit board design criteria

Parameter	Description
Maximum circuit board thickness	3.81 mm (0.150 in)
Footprint type	PCI Express Gen1 or Gen2
Pad finish	Immersion gold over nickel (immersion silver and hot air solder level (HASL) also acceptable)

NOTE. *Tektronix recommends that the holes made for the retention mechanism posts remain unconnected to a ground plane. This prevents overheating the ground plane and promotes quicker soldering of the retention posts to your PCB.*

Footprint dimensions and keep-out area. Design your circuit board layout using the following footprint dimensions so that a probe retention mechanism will fit properly and make good electrical contact with your system. (See Figure 20 on page 22.) The space around the footprint (keep-out area) represents the area that will be covered by the retention mechanism.

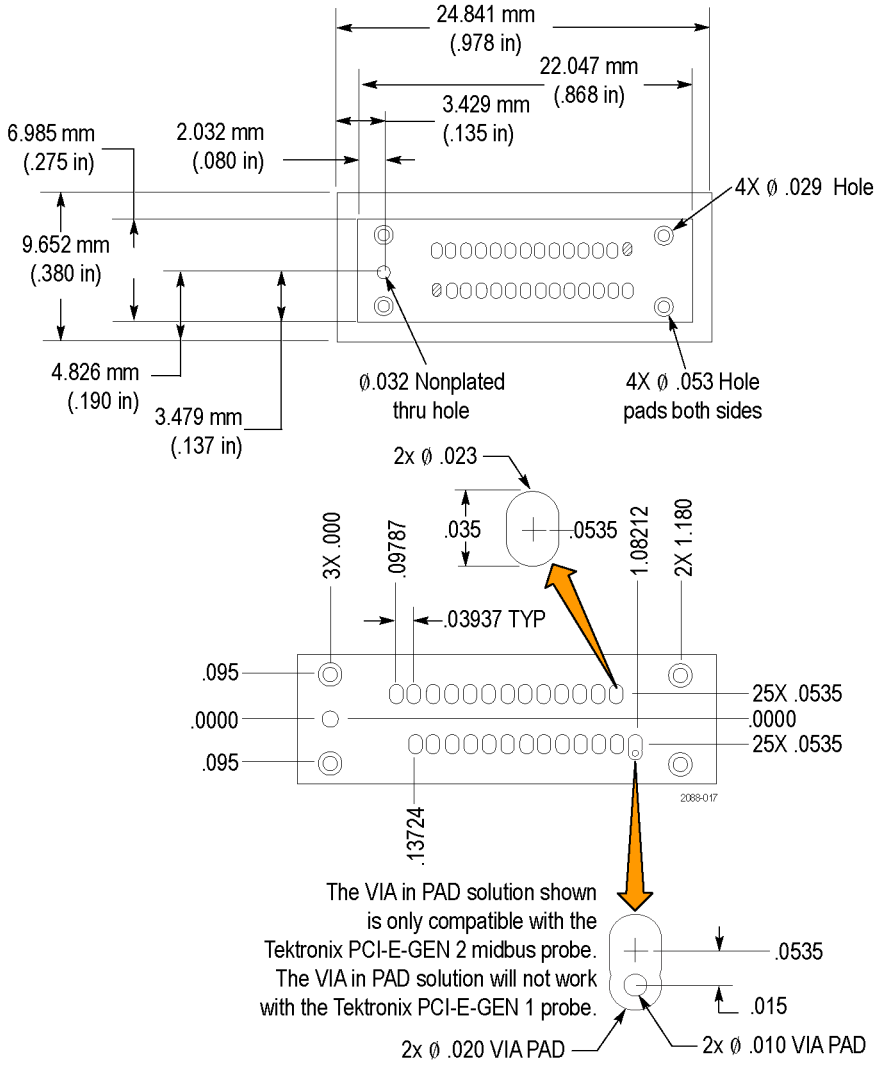


Figure 20: 8-Channel mid-bus footprint dimensions and keep-out area

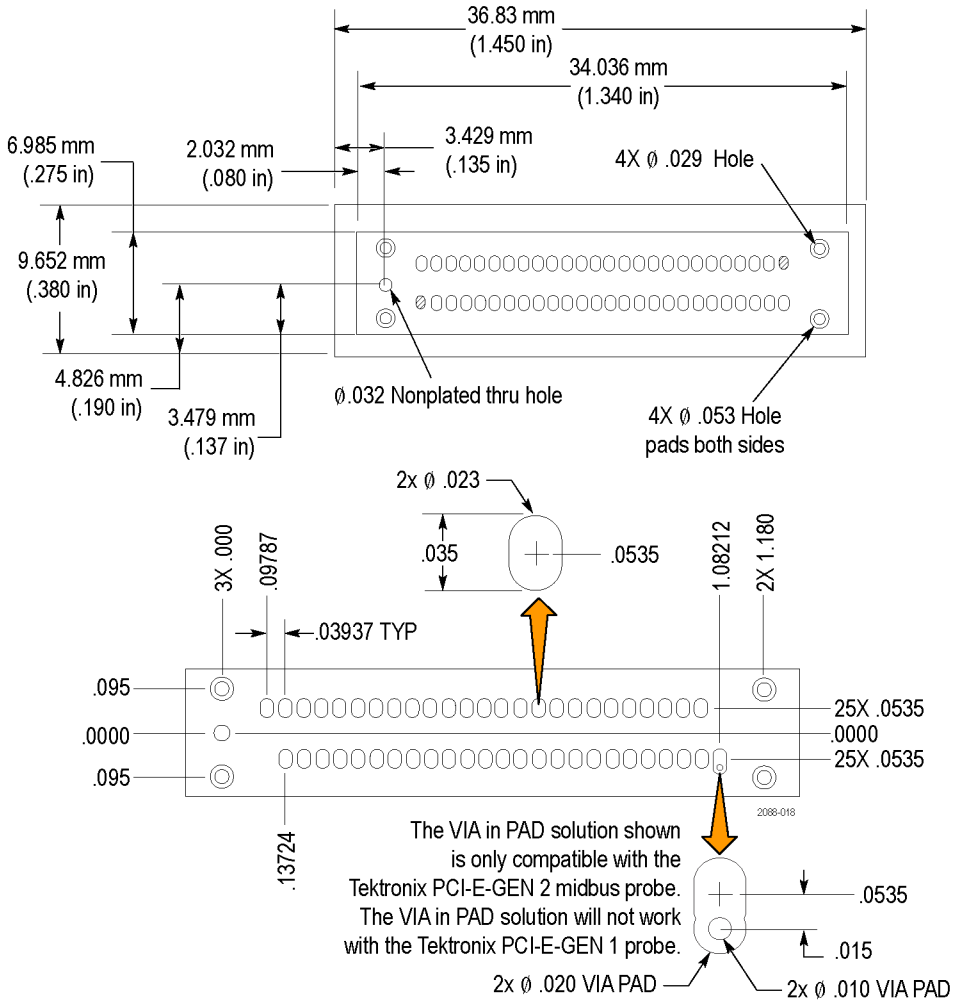


Figure 21: 16-Channel mid-bus footprint dimensions and keep-out area

Routing Considerations for the Mid-bus Probe Footprint. Routing and simulation studies have been performed near and through the PCI Express mid-bus footprint to determine a best known method for maintaining integrity of the system channel as well as provide an adequate signal to the serial analyzer. However, the following information does not imply that superior routing techniques do not exist. It is mandatory that you closely monitor and simulate the routing near and through the mid-bus probe to insure that integrity of the system and mid-bus signal eye are maximized. Some dimensional details concluded from these simulations and studies are provided in the following table.

NOTE. *The via hole size in the following table is a minimum size, based on the assumption that the circuit board is 2.36 mm (0.093-inch) thick.*

Table 2: Via and trace characteristics

Parameter	Size
Via hole	10 mil
Via annular ring	20 mil
Via antipad	33 mil
Minimum space between via annular ring and pad	5 mil
Trace width	14 mil
Microtrace width	5 mil
Space between traces (before and after footprint negotiation)	14 mil
Space between microtraces (before and after footprint negotiation)	5 mil

Primary Surface Layer Routing. The following figure shows recommended trace routing on the primary surface layer (the surface where the mid-bus footprint will be). The solid white pads shown in the diagram are the ground pads.

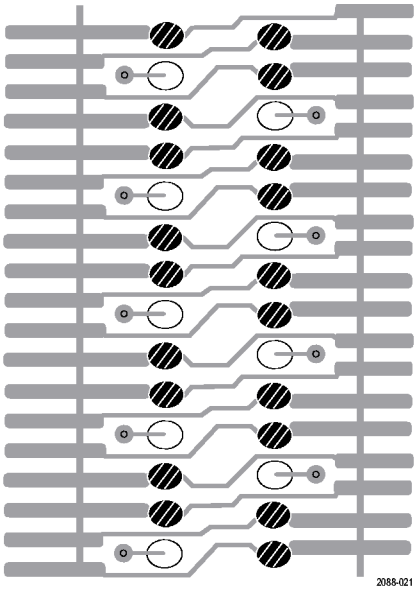


Figure 22: Recommended trace routing on primary surface layer

Tektronix recommends that you design your footprint so that there are no traces or vias in the two spaces designated in the following diagram. If your design requires the use of these two spaces, Tektronix recommends that you fully solder mask these areas.

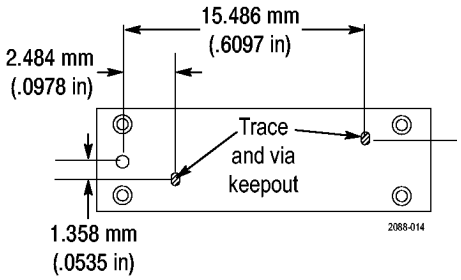


Figure 23: Via and trace keep-out areas for the P6708 8-Channel probe

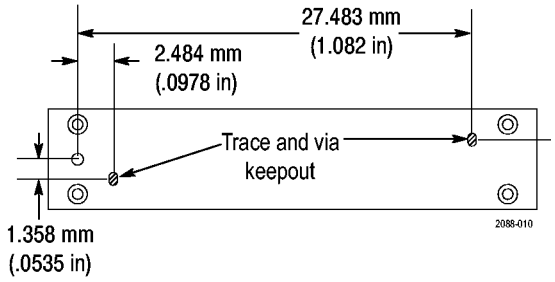


Figure 24: Via and trace keep-out areas for the P6716 16-Channel probe

Inner Layer or Secondary Surface Layer Routing. The following figures show suggested trace routing on the inner layer, and the secondary surface layer (the surface opposite from where the mid-bus footprint will be). The solid white pads shown in the diagram are the ground pads.

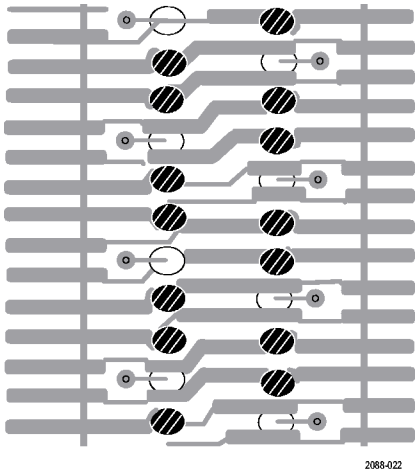


Figure 25: Recommended trace routing on inner or secondary surface layer (primary layer pads shown)

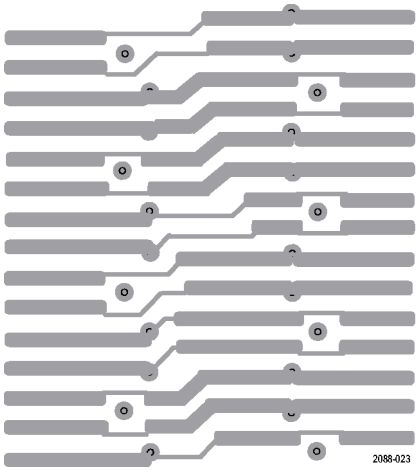


Figure 26: Recommended trace routing on inner or secondary surface layer (primary layer pads not shown)

Clock Cable Three-Pin Connector

If you intend to use a mid-bus probe and a clock cable, a three-pin micro-terminal strip connector must be installed on your SUT. A non-intrusive clock cable (Tektronix part number, 672-6285-00) has two SMA connectors on one end (+ and –), and a small circuit board with a mating three-pin connector on the other. Only one connector is needed, even if more than one TLA7Sxx module is used. In this case, a "jumper" clock cable with SMA connectors on each end (+ and –) can connect the two modules and share the clock signal.

Tektronix suggests installing the following three-pin connector (or similar):

- Through hole: Samtec® TMS 103-02-S-S

  (1 x 3, 0.05 center spacing)

- Surface mount: Samtec® FTR 103-02-S-S

  (1 x 3, 0.05 center spacing)

Table 3: Clock cable three-pin connector pin assignments

Signal	Pin number
REFCLKp	1 (or 3) [1]
GND	2
REFCLKn	3 (or 1) [1]

[1] The serial analyzer module is not sensitive to the polarity of the reference clock signal. The clock cable connector can be attached in either orientation.

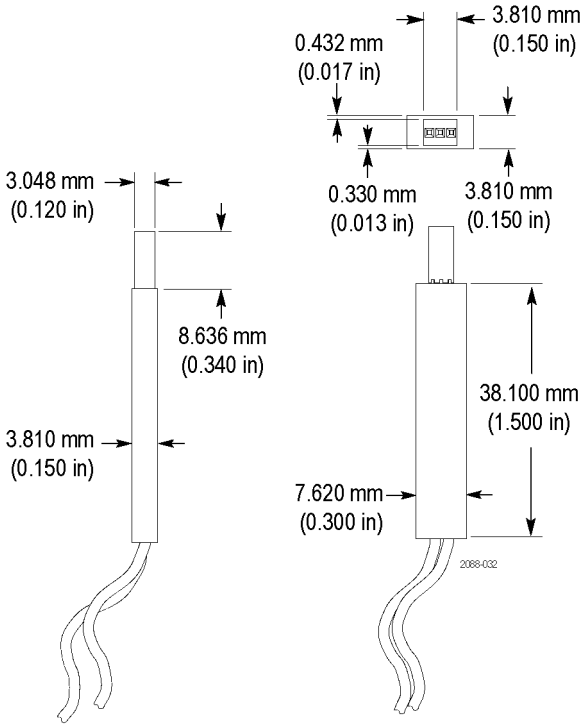


Figure 27: Clock cable connector dimensions

For more specific information on keep-out volumes for particular system configurations, contact your local Tektronix representative.

P6701SD Probe Solder Tip (P75TLRST)

The P75TLRST probe tip is designed for solder-down probing applications. It is composed of a small form factor interconnect circuit board with SMD0402 damping resistors and a set of vias for wire attachment to the SUT. The circuit board vias are designed for both 4 mil and 8 mil wire and a special high tensile strength wire is supplied as part of the wire accessory kit. The expanded view of the probe tip shows the location of the + and – signal inputs as well as the two ground reference connections. (See Figure 28.)

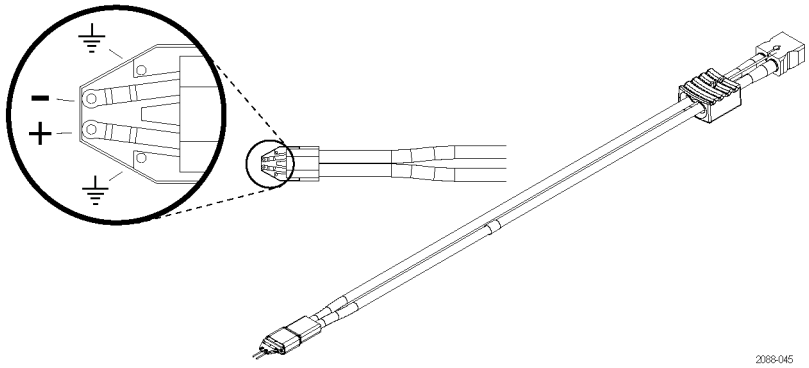


Figure 28: P75TLRST TriMode Long Reach Solder Tip

Attached to the circuit board are a pair of very low skew (<1ps) coaxial cables and a polarized G3PO dual connector block. The 3GPO connectors use a miniature, high frequency design that enables quick and easy installation of the P75TLRST solder tip. The G3PO connector block of the probe tip is inserted into the input nose piece on the end of the P6701SD Serial Analyzer probe body. The probe body contains a mating, polarized G3PO connector block with attached G3PO connector bullets.

The connector bullets are a part of the G3PO connector design, providing a self-aligning interconnect mechanism between G3PO connectors. The G3PO connector in the probe body is designed to have higher detent force than the probe tip connectors, which is intended to ensure that the G3PO bullets remain in the probe body connector when disconnected.

The probe body nose piece, with its integral spring mechanism, helps to provide a self-aligning mechanism for hand insertion of the probe tip. The probe body nose springs also give a secure capture of the probe tip connector after insertion.

Release of the probe tip is assisted by using the wire-connected cable release holder on the probe tip connector. This probe tip release holder should always be used rather than pulling on the probe tip cables, which may cause tip cable damage.

The recommended wire attachment method is to first solder the wires to the SUT, being careful to minimize the wire length of the signal and ground connections. This is followed by threading the wires through the probe tip board vias, being careful to achieve as symmetrical a wire pattern as possible between the two signal inputs and a very short ground connection.

Finally, the attachment is completed by soldering the wires on top of the probe tip circuit board. Any excess wire lead length extending through the probe tip board should be removed to minimize possible signal reflection problems. Because of the limited mechanical strength of the wire interconnect and probe tip circuit board, the solder-down probe tip should be taped down at the SUT for strain relief. Although the accessory kit includes adhesive strips that can be used for the strain relief of the probe tip, the use of mylar tape will generally provide stronger attachment if room is available at the SUT.

The lead length of the connection wires between the probe tip board and the SUT must be kept as short as possible to preserve the integrity of the measured signal. Typical wire lengths range from 0.010 in. to 0.100 in. (See Figure 29.)

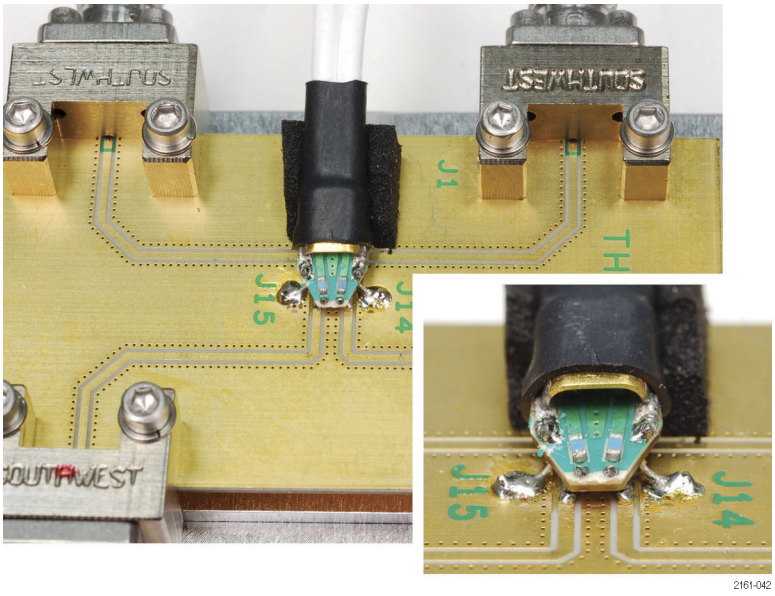


Figure 29: Typical wire length from probe tip to circuit

The following four figures illustrate the signal integrity effect on the P75TLRST solder tip when used with different lengths of tip wire. Signal fidelity is best when the wire length is kept as short as possible. The step generator that was used as a signal source for these screenshots has a 30 ps 10-90% rise time. The table in each figure contains data for two rise time measurements (10-90% and 20-80%).

These screenshots can be used as a guide to gauge the effects of wire length, but actual results may vary depending on the other factors like characteristics of the device under test (for example, rise time and impedance), and the precision of the solder connection.

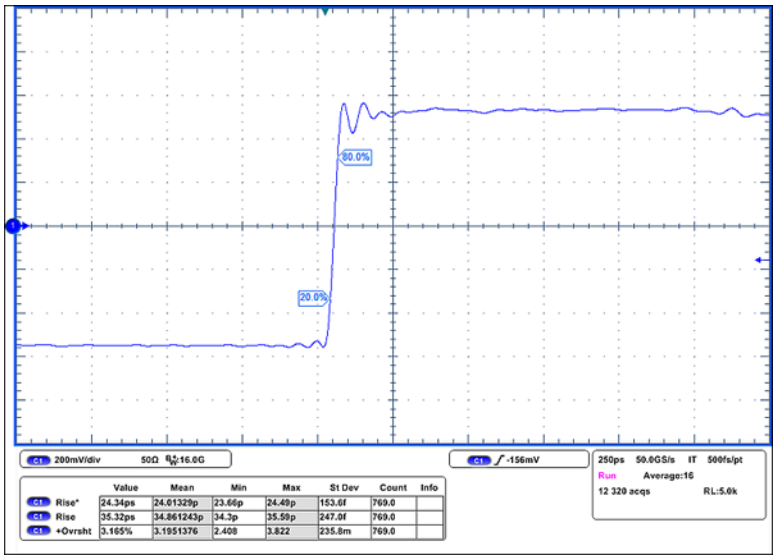


Figure 30: P75TLRST solder tip with 0.010 inch of tip wire

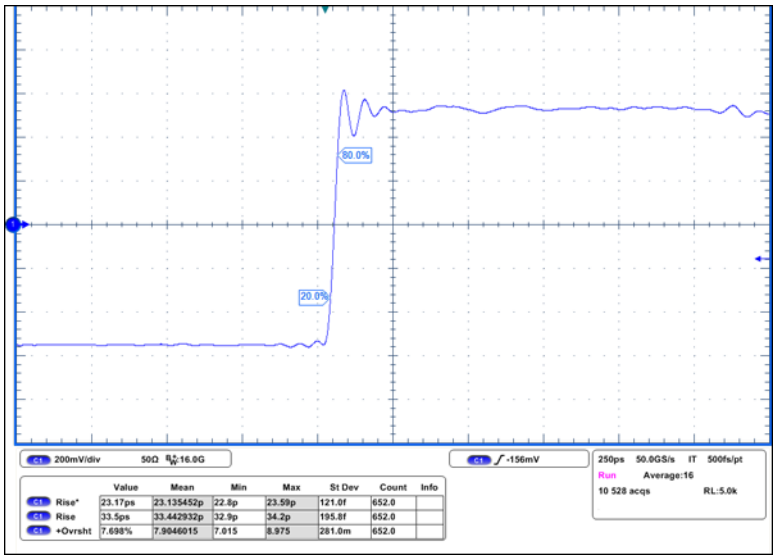


Figure 31: P75TLRST solder tip with 0.050 inch of tip wire

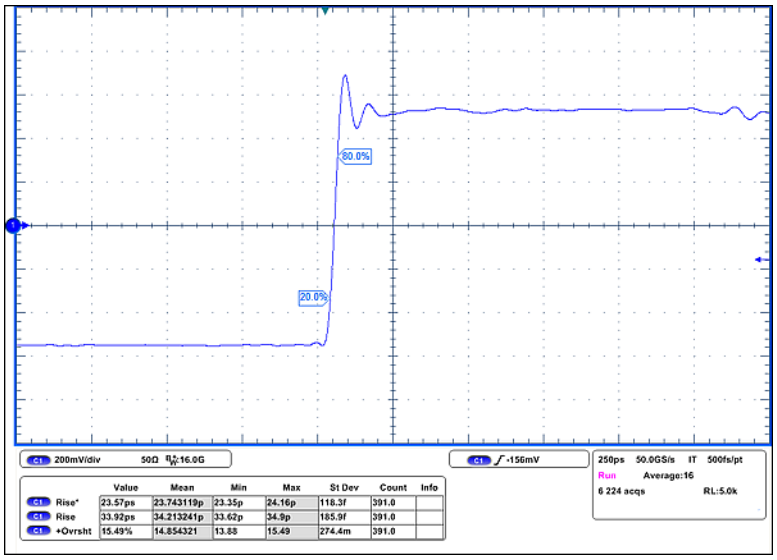


Figure 32: P75TLRST solder tip with 0.100 inch of tip wire

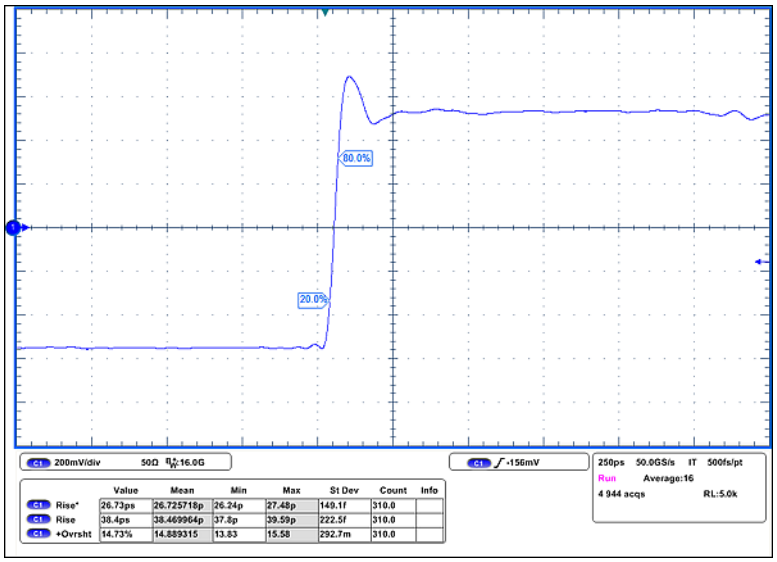


Figure 33: P75TLRST solder tip with 0.200 inch of tip wire

The following figure shows the dimensions of the P75TLRST Solder Tip.

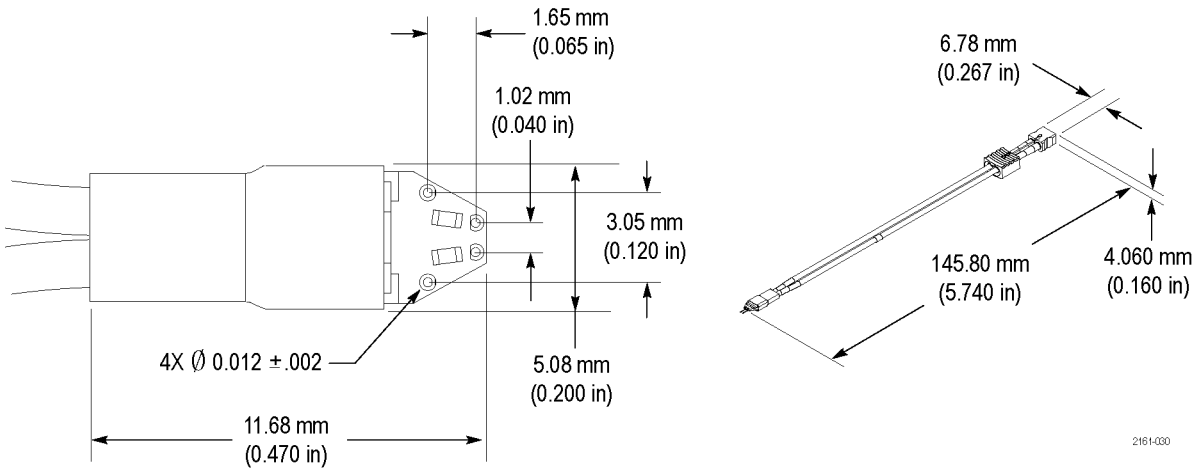


Figure 34: P75TLRST TriMode Long Reach Solder Tip dimensions

Electrical Design

For the serial analyzer module to reliably capture logical transactions on the bus, adequate signal eye must be available at the mid-bus footprint while the probe is connected. This must be verified by electrical simulation using the load model of the P67xx Series probe. (See Figure 36 on page 35.)

Eye requirements are defined at the mid-bus footprint (or at the solder tip input for the P6701SD probe) and are measured by eye height and eye width, forming a diamond shape.

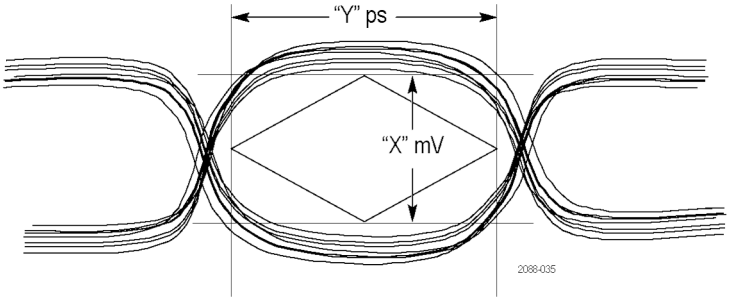


Figure 35: Signal eye measurements (time vs voltage)

The following specifications limit the electrical distance between the driver pin and the mid-bus footprint. When analyzing both directions of an electrically long PCI Express link, you might need to design your system with two separate footprints to maintain adequate signal eye. Eye requirements apply regardless of circuit board material and infrastructure.

Table 4: Mid-bus Probe Eye Requirements

Parameter	Description [1] [3]
Minimum Eye Height at footprint pad [1]	45 mV
Unit Interval Gen1	400 ps
Unit Interval Gen2	200 ps
Minimum Eye Width at midbus pad	0.7 UI [2]

1 Eye Height/Width values apply to both data rates.

2 Does not include jitter at frequencies below 10 MHz.

3 Measurements include random jitter of 5 ps RMS

Table 5: Solder-Down Probe Eye Requirements

Parameter	Description [1] [3]
Minimum Eye Height at solder tip input [1]	60 mV
Unit Interval Gen1	400 ps
Unit Interval Gen2	200 ps
Minimum Eye Width at solder tip input	0.7 UI [2]

1 Eye Height/Width values apply to both data rates.

2 Does not include jitter at frequencies below 10 MHz.

3 Measurements include random jitter of 5 ps RMS

Measuring signal eye. Tektronix recommends using a TDS6154C oscilloscope with a P7500 series probe with solder-down tips for most accurate results. If your system does not allow you to use solder-down tips, use the handheld Precision Differential Probing Module (Tektronix part number P75PDPM). Tektronix recommends using TDSJIT3 Advanced software to take signal eye measurements. Tektronix RT-Eye software is also acceptable. For instructions on using TDSJIT3 Advanced and RT Eye software, go to Tektronix.com/manuals, or contact your local Tektronix representative.

P67xx Series mid-bus probe circuit impact. Tektronix has provided two Touchstone® models (sdd12wop.dat and sdd12wp.dat). (See page 71, *Reference Files*.) These models simulate the impact of the P67xx Series mid-bus probe (8 or 16 channel) retention mechanisms with and without the probe installed. This is actual S-parameter measured data using real probes and retentions. Graphical representation of the data is provided in the next two graphs.

The first graph shows the frequency response of a transmission line loaded with a P67xx mid-bus probe retention. (See Figure 36 on page 35.)

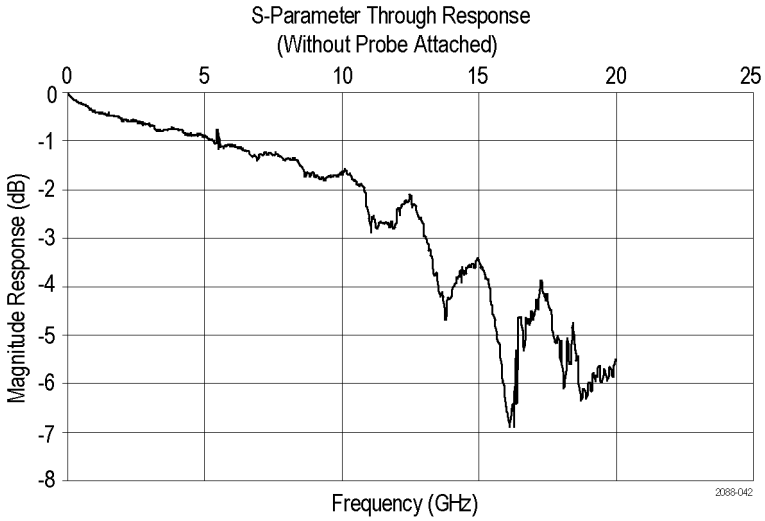


Figure 36: S-parameter data of retention mechanism only

The second graph shows the frequency response of a transmission line loaded with a P67xx mid-bus probe retention and a probe. (See Figure 38.)

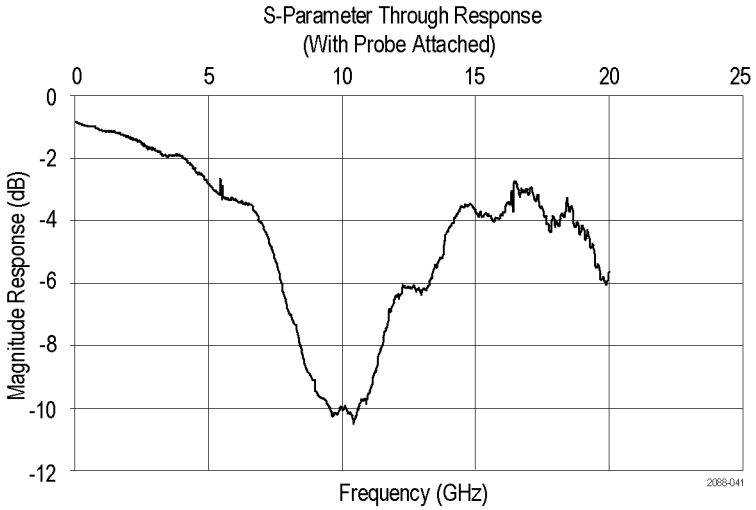


Figure 37: S-parameter data of retention mechanism plus P67xx Series mid-bus probe

P67xxS Series Slot Interposer Probe circuit impact. Tektronix has provided Touchstone® models to simulate the impact of a P67xxS Series slot interposer probe. (See page 71, *Reference Files*.) This is actual S-parameter measured data using a real P67xxS interposer probe.

P6701SD Solder-Down Probe circuit impact. Tektronix has provided a Touchstone® model (P6701SD.dat) to simulate the impact of a P6701SD solder-down probe and P75TLRST solder tip.. (See page 71, *Reference Files*.) This is actual S-parameter measured data using a real P6701SD solder-down probe. Graphical representation of the data is provided in the following graph. It shows the frequency response of a transmission line loaded with a P6701SD solder-down probe and P75TLRST solder tip.

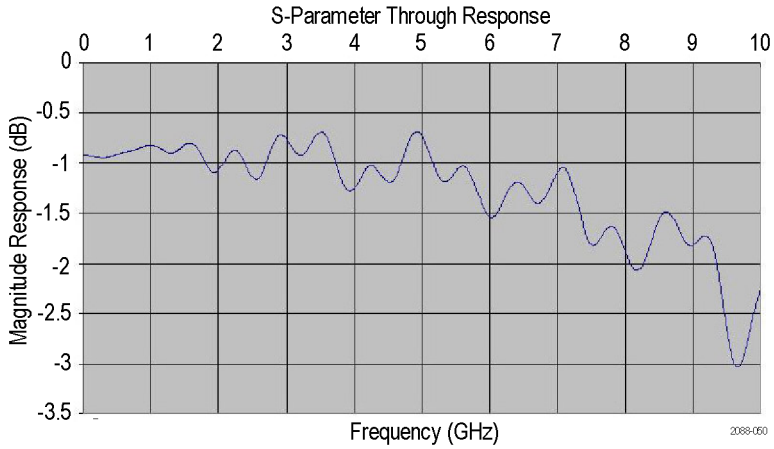


Figure 38: S-parameter data of P6701SD Solder-Down probe

Reference Clock Signal

The TLA7S08 & TLA7S16 Serial Analyzer modules can recognize a clock signal from a cable connection to the SUT, or by recovering the clock signal embedded in the data.

Recognize the clock signal embedded in the data stream. A stable reference signal is generated by the serial analyzer and synchronized with the embedded clock signal. A clock cable connection is not required, since the logic analyzer recognizes the embedded signal from the probe.

The transfer rate of the serial link must be 2.5 GT/s ± 300 ppm (PCI Express Gen 1) or 5.0 GT/s ± 300 ppm (PCI Express Gen 2). If the transfer rate is not within this range, the module will not capture the data reliably.

If SSC (spread spectrum clocking) is enabled, and your PCI Express link uses power management states, you must connect a clock cable to the SUT and set the reference clock source to SUT so that the module will capture data reliably.

Recognize the clock signal by directly connecting to the SUT with a clock cable. Tektronix recommends connecting a clock cable to ensure that data is accurately synchronized with the clock signal.

If you intend to use a mid-bus probe, you must install a three-pin connector on your SUT to connect to the clock cable. (See page 26, *Clock Cable Three-Pin Connector*.) Slot interposer probes already have this connector installed on the probe.

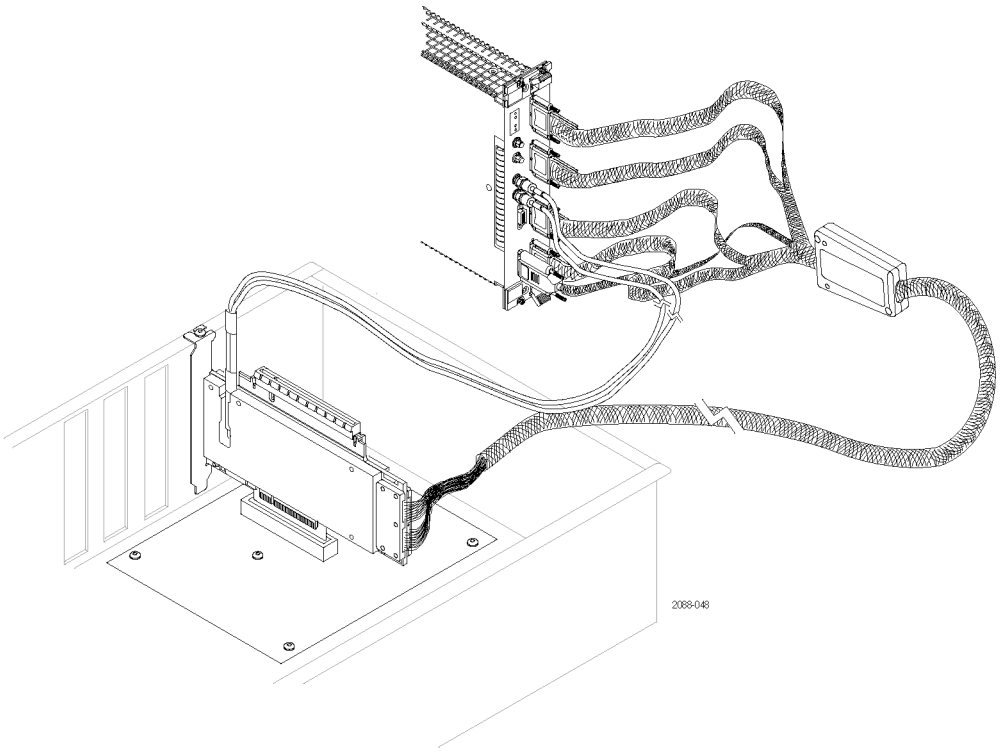


Figure 39: Slot Interposer probe with a clock cable connected

Table 6: Reference clock electrical requirements

Serial module requirement	Symbol	Minimum	Typical	Maximum
Differential Voltage at Ref Clock Attach Point	Vdiff [2]	0.8 V	-	2.0 V
Absolute Voltage Limit at Ref Clock Attach Point	Vabs	0 V	-	3.3 V
Reference Clock Frequency –100 MHz	Freq100	-	100 MHz +/-300 ppm	-
Reference Clock Frequency –100 MHz + 10% [1]	Freq100 +10%	-	110 MHz +/-300 ppm	-
Reference Clock Frequency –100 MHz - 10% [1]	Freq100 -10%	-	90 MHz +/-300 ppm	-
Reference Clock Frequency –125 MHz [1]	Freq125	-	125 MHz +/-300 ppm	-
Reference Clock Total Jitter	RefClkJitter	- -	<1 MHz: 25 ps p-p >1 MHz: 200 ps p-p	- -

1 With SSC (spread spectrum clocking) enabled or disabled

2 Vdiff= |2*(Vrefclockp - Vrefclockn)|

3 Peak to peak

Mid-bus Footprint Pin and Probe Channel Assignments

The following figure shows the standard pin assignments for a PCI Express 8-channel footprint.

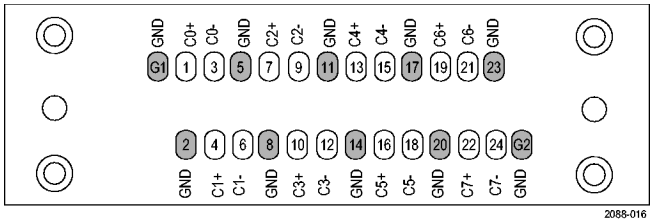


Figure 40: P6708 8-Channel probe footprint pin assignments

The following figure shows the standard pin assignments for a PCI Express 16-channel footprint.

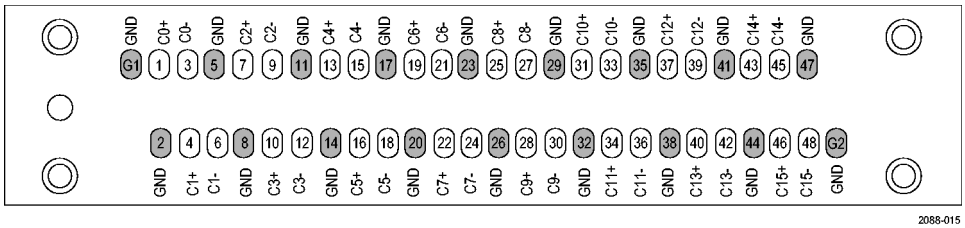


Figure 41: P6716 16-Channel probe footprint pin assignments

General Guidelines for Pin-Channel Assignment

Tektronix strongly recommends that you design your system so that pins are assigned to channels according to the following guidelines and the standard formats listed in the tables. The formats listed in the tables were created so that each module-end probe connector contains the wires connected to adjacent differential pairs on the footprint.

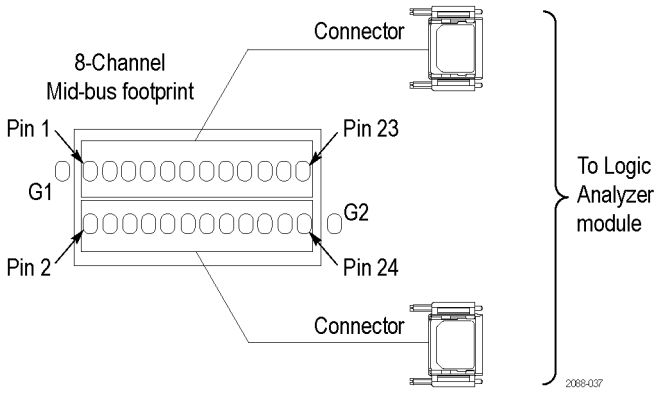


Figure 42: 8-Channel mid-bus footprint connection module connector

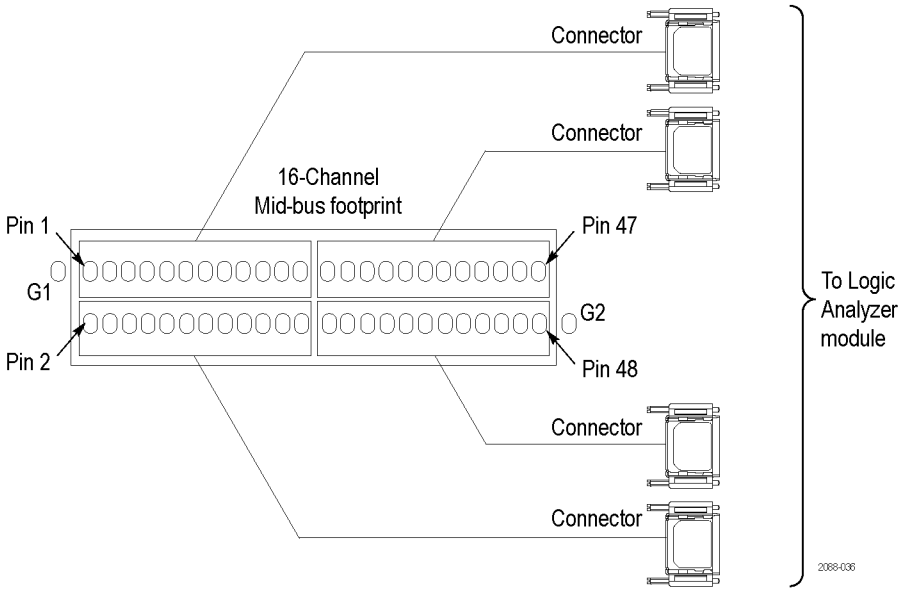


Figure 43: 16-Channel mid-bus footprint connection module connector

The serial analyzer software is designed to be easily configured based on these standard formats. If your system design does not allow you to follow these guidelines, or if a footprint is incorrectly wired, you may have to disassemble and rewire the connector at the module end of the probe. (See page 54, *Rearranging Wires in the Probe Connector*.)

- The differential pairs that make up a PCI Express link must be connected to specific pads (pins) on the footprint
- The polarity of the differential pairs can be swapped, if required, for routing
- Upstream and downstream channels can be swapped on a footprint, if required, for routing
- Entire links can be reversed compared to the suggested routing

Key concepts for the channel mapping tables.

- Each channel is connected to either an upstream OR downstream differential pair.
- Signal name = C[*number*][*p* (positive) or *n* (negative)]

  Example: C3p = the positive signal of the differential pair connected to channel three

The following tables show footprint pin-channel assignments for PCI Express links of various standard recommended configurations.

16-Channel PCI Express Mid-bus Pin Assignments

Table 7: X16 unidirectional link

Pin #	Signal name	Pin #	Signal name
		G1	GND
2	GND	1	C0p
4	C1p	3	C0n
6	C1n	5	GND
8	GND	7	C2p
10	C3p	9	C2n
12	C3n	11	GND
14	GND	13	C4p
16	C5p	15	C4n
18	C5n	17	GND
20	GND	19	C6p
22	C7p	21	C6n
24	C7n	23	GND
26	GND	25	C8p
28	C9p	27	C8n
30	C9n	29	GND
32	GND	31	C10p
34	C11p	33	C10n
36	C11n	35	GND
38	GND	37	C12p
40	C13p	39	C12n
42	C13n	41	GND
44	GND	43	C14p
46	C15p	45	C14n
48	C15n	47	GND
G2	GND		

Table 8: X8 bidirectional link

Pin #	Signal name	Pin #	Signal name
		G1	GND
2	GND	1	C0p- Upstream
4	C0p- Downstream	3	C0n- Upstream
6	C0n- Downstream	5	GND
8	GND	7	C1p- Upstream
10	C1p- Downstream	9	C1n- Upstream
12	C1n- Downstream	11	GND
14	GND	13	C2p- Upstream
16	C2p- Downstream	15	C2n- Upstream
18	C2n- Downstream	17	GND
20	GND	19	C3p- Upstream
22	C3p- Downstream	21	C3n- Upstream
24	C3n- Downstream	23	GND
26	GND	25	C4p- Upstream
28	C4p- Downstream	27	C4n- Upstream
30	C4n- Downstream	29	GND
32	GND	31	C5p- Upstream
34	C5p- Downstream	33	C5n- Upstream
36	C5n- Downstream	35	GND
38	GND	37	C6p- Upstream
40	C6p- Downstream	39	C6n- Upstream
42	C6n- Downstream	41	GND
44	GND	43	C7p- Upstream
46	C7p- Downstream	45	C7n- Upstream
48	C7n- Downstream	47	GND
G2	GND		

Table 9: X8 (2) unidirectional links

Pin #	Signal name	Pin #	Signal name
		G1	GND
2	GND	1	C0p- DirectionA
4	C1p- DirectionA	3	C0n- DirectionA
6	C1n- DirectionA	5	GND
8	GND	7	C2p- DirectionA
10	C3p- DirectionA	9	C2n- DirectionA
12	C3n- DirectionA	11	GND
14	GND	13	C4p- DirectionA
16	C5p- DirectionA	15	C4n- DirectionA
18	C5n- DirectionA	17	GND
20	GND	19	C6p- DirectionA
22	C7p- DirectionA	21	C6n- DirectionA
24	C7n- DirectionA	23	GND
26	GND	25	C0p- DirectionB
28	C1p- DirectionB	27	C0n- DirectionB
30	C1n- DirectionB	29	GND
32	GND	31	C2p- DirectionB
34	C3p- DirectionB	33	C2n- DirectionB
36	C3n- DirectionB	35	GND
38	GND	37	C4p- DirectionB
40	C5p- DirectionB	39	C4n- DirectionB
42	C5n- DirectionB	41	GND
44	GND	43	C6p- DirectionB
46	C7p- DirectionB	45	C6n- DirectionB
48	C7n- DirectionB	47	GND
G2	GND		

Table 10: X4 bidirectional link

Pin #	Signal name	Pin #	Signal name
		G1	GND
2	GND	1	C0p- Upstream1
4	C0p- Downstream1	3	C0n- Upstream1
6	C0n- Downstream1	5	GND
8	GND	7	C1p- Upstream1
10	C1p- Downstream1	9	C1n- Upstream1
12	C1n- Downstream1	11	GND
14	GND	13	C2p- Upstream1
16	C2p- Downstream1	15	C2n- Upstream1
18	C2n- Downstream1	17	GND
20	GND	19	C3p- Upstream1
22	C3p- Downstream1	21	C3n- Upstream1
24	C3n- Downstream1	23	GND
26	GND	25	C0p- Upstream2
28	C0p- Downstream2	27	C0n- Upstream2
30	C0n- Downstream2	29	GND
32	GND	31	C1p- Upstream2
34	C1p- Downstream2	33	C1n- Upstream2
36	C1n- Downstream2	35	GND
38	GND	37	C2p- Upstream2
40	C2p- Downstream2	39	C2n- Upstream2
42	C2n- Downstream2	41	GND
44	GND	43	C3p- Upstream2
46	C3p- Downstream2	45	C3n- Upstream2
48	C3n- Downstream2	47	GND
G2	GND		

Table 11: X4 (2) unidirectional links

Pin #	Signal name	Pin #	Signal name
		G1	GND
2	GND	1	C0p- DirectionA
4	C1p- DirectionA	3	C0n- DirectionA
6	C1n- DirectionA	5	GND
8	GND	7	C2p- DirectionA
10	C3p- DirectionA	9	C2n- DirectionA
12	C3n- DirectionA	11	GND
14	GND	13	Not connected
16	Not connected	15	Not connected
18	Not connected	17	GND
20	GND	19	Not connected
22	Not connected	21	Not connected
24	Not connected	23	GND
26	GND	25	C0p- DirectionB
28	C1p- DirectionB	27	C0n- DirectionB
30	C1n- DirectionB	29	GND
32	GND	31	C2p- DirectionB
34	C3p- DirectionB	33	C2n- DirectionB
36	C3n- DirectionB	35	GND
38	GND	37	Not connected
40	Not connected	39	Not connected
42	Not connected	41	GND
44	GND	43	Not connected
46	Not connected	45	Not connected
48	Not connected	47	GND
G2	GND		

Table 12: X2 bidirectional link

Pin #	Signal name	Pin #	Signal name
		G1	GND
2	GND	1	C0p- Upstream1
4	C0p- Downstream1	3	C0n- Upstream1
6	C0n- Downstream1	5	GND
8	GND	7	C1p- Upstream1
10	C1p- Downstream1	9	C1n- Upstream1
12	C1n- Downstream1	11	GND
14	GND	13	Not connected
16	Not connected	15	Not connected
18	Not connected	17	GND
20	GND	19	Not connected
22	Not connected	21	Not connected
24	Not connected	23	GND
26	GND	25	C0p- Upstream2
28	C0p- Downstream2	27	C0n- Upstream2
30	C0n- Downstream2	29	GND
32	GND	31	C1p- Upstream2
34	C1p- Downstream2	33	C1n- Upstream2
36	C1n- Downstream2	35	GND
38	GND	37	Not connected
40	Not connected	39	Not connected
42	Not connected	41	GND
44	GND	43	Not connected
46	Not connected	45	Not connected
48	Not connected	47	GND
G2	GND		

Table 13: X2 (2) unidirectional links

Pin #	Signal name	Pin #	Signal name
		G1	GND
2	GND	1	C0p- DirectionA
4	C1p- DirectionA	3	C0n- DirectionA
6	C1n- DirectionA	5	GND
8	GND	7	Not connected
10	Not connected	9	Not connected
12	Not connected	11	GND
14	GND	13	Not connected
16	Not connected	15	Not connected
18	Not connected	17	GND
20	GND	19	Not connected
22	Not connected	21	Not connected
24	Not connected	23	GND
26	GND	25	C0p- DirectionB
28	C1p- DirectionB	27	C0n- DirectionB
30	C1n- DirectionB	29	GND
32	GND	31	Not connected
34	Not connected	33	Not connected
36	Not connected	35	GND
38	GND	37	Not connected
40	Not connected	39	Not connected
42	Not connected	41	GND
44	GND	43	Not connected
46	Not connected	45	Not connected
48	Not connected	47	GND
G2	GND		

Table 14: X1 bidirectional link

Pin #	Signal name	Pin #	Signal name
		G1	GND
2	GND	1	C0p- Upstream1
4	C0p- Downstream1	3	C0n- Upstream1
6	C0n- Downstream1	5	GND
8	GND	7	Not connected
10	Not connected	9	Not connected
12	Not connected	11	GND
14	GND	13	Not connected
16	Not connected	15	Not connected
18	Not connected	17	GND
20	GND	19	Not connected
22	Not connected	21	Not connected
24	Not connected	23	GND
26	GND	25	C0p- Upstream2
28	C0p- Downstream2	27	C0n- Upstream2
30	C0n- Downstream2	29	GND
32	GND	31	Not connected
34	Not connected	33	Not connected
36	Not connected	35	GND
38	GND	37	Not connected
40	Not connected	39	Not connected
42	Not connected	41	GND
44	GND	43	Not connected
46	Not connected	45	Not connected
48	Not connected	47	GND
G2	GND		

Table 15: X1 (2) unidirectional links

Pin #	Signal name	Pin #	Signal name
		G1	GND
2	GND	1	C0p- DirectionA
4	Not connected	3	C0n- DirectionA
6	Not connected	5	GND
8	GND	7	Not connected
10	Not connected	9	Not connected
12	Not connected	11	GND
14	GND	13	Not connected
16	Not connected	15	Not connected
18	Not connected	17	GND
20	GND	19	Not connected
22	Not connected	21	Not connected
24	Not connected	23	GND
26	GND	25	C0p- DirectionB
28	Not connected	27	C0n- DirectionB
30	Not connected	29	GND
32	GND	31	Not connected
34	Not connected	33	Not connected
36	Not connected	35	GND
38	GND	37	Not connected
40	Not connected	39	Not connected
42	Not connected	41	GND
44	GND	43	Not connected
46	Not connected	45	Not connected
48	Not connected	47	GND
G2	GND		

8-Channel PCI Express Mid-bus Pin Assignments

Table 16: X8 unidirectional link

Pin #	Signal name	Pin #	Signal name
2	GND	1	C0p- DirectionA
4	C1p- DirectionA	3	C0n- DirectionA
6	C1n- DirectionA	5	GND
8	GND	7	C2p- DirectionA
10	C3p- DirectionA	9	C2n- DirectionA
12	C3n- DirectionA	11	GND
14	GND	13	C4p- DirectionA
16	C5p- DirectionA	15	C4n- DirectionA
18	C5n- DirectionA	17	GND
20	GND	19	C6p- DirectionA
22	C7p- DirectionA	21	C6n- DirectionA
24	C7n- DirectionA	23	GND

Table 17: X4 bidirectional link

Pin #	Signal name	Pin #	Signal name
2	GND	1	C0p- Upstream
4	C0p- Downstream	3	C0n- Upstream
6	C0n- Downstream	5	GND
8	GND	7	C1p- Upstream
10	C1p- Downstream	9	C1n- Upstream
12	C1n- Downstream	11	GND
14	GND	13	C2p- Upstream
16	C2p- Downstream	15	C2n- Upstream
18	C2n- Downstream	17	GND
20	GND	19	C3p- Upstream
22	C3p- Downstream	21	C3n- Upstream
24	C3n- Downstream	23	GND

Table 18: X4 (2) unidirectional links

Pin #	Signal name	Pin #	Signal name
2	GND	1	C0p- DirectionA
4	C1p- DirectionA	3	C0n- DirectionA
6	C1n- DirectionA	5	GND
8	GND	7	C2p- DirectionA
10	C3p- DirectionA	9	C2n- DirectionA
12	C3n- DirectionA	11	GND
14	GND	13	C0p- DirectionB
16	C1p- DirectionB	15	C0n- DirectionB
18	C1n- DirectionB	17	GND
20	GND	19	C2p- DirectionB
22	C3p- DirectionB	21	C2n- DirectionB
24	C3n- DirectionB	23	GND

Table 19: X4 unidirectional link and a X2 unidirectional link

Pin #	Signal name	Pin #	Signal name
2	GND	1	C0p- DirectionA
4	C1p- DirectionA	3	C0n- DirectionA
6	C1n- DirectionA	5	GND
8	GND	7	C2p- DirectionA
10	C3p- DirectionA	9	C2n- DirectionA
12	C3n- DirectionA	11	GND
14	GND	13	C0p- DirectionB
16	C1p- DirectionB	15	C0n- DirectionB
18	C1n- DirectionB	17	GND
20	GND	19	Not connected
22	Not connected	21	Not connected
24	Not connected	23	GND

Table 20: X4 unidirectional link and a X1 unidirectional link

Pin #	Signal name	Pin #	Signal name
2	GND	1	C0p- DirectionA
4	C1p- DirectionA	3	C0n- DirectionA
6	C1n- DirectionA	5	GND
8	GND	7	C2p- DirectionA
10	C3p- DirectionA	9	C2n- DirectionA
12	C3n- DirectionA	11	GND
14	GND	13	C0p- DirectionB
16	Not connected	15	C0n- DirectionB
18	Not connected	17	GND
20	GND	19	Not connected
22	Not connected	21	Not connected
24	Not connected	23	GND

Table 21: X2 bidirectional link

Pin #	Signal name	Pin #	Signal name
2	GND	1	C0p- Upstream1
4	C0p- Downstream1	3	C0n- Upstream1
6	C0n- Downstream1	5	GND
8	GND	7	C1p- Upstream1
10	C1p- Downstream1	9	C1n- Upstream1
12	C1n- Downstream1	11	GND
14	GND	13	C0p- Upstream2
16	C0p- Downstream2	15	C0n- Upstream2
18	C0n- Downstream2	17	GND
20	GND	19	C1p- Upstream2
22	C1p- Downstream2	21	C1n- Upstream2
24	C1n- Downstream2	23	GND

Table 22: X2 (2) unidirectional links

Pin #	Signal name	Pin #	Signal name
2	GND	1	C0p- DirectionA
4	C1p- DirectionA	3	C0n- DirectionA
6	C1n- DirectionA	5	GND
8	GND	7	Not connected
10	Not connected	9	Not connected
12	Not connected	11	GND
14	GND	13	C0p- DirectionB
16	C1p- DirectionB	15	C0n- DirectionB
18	C1n- DirectionB	17	GND
20	GND	19	Not connected
22	Not connected	21	Not connected
24	Not connected	23	GND

Table 23: X1 bidirectional link

Pin #	Signal name	Pin #	Signal name
2	GND	1	C0p- Upstream1
4	C0p- Downstream1	3	C0n- Upstream1
6	C0n- Downstream1	5	GND
8	GND	7	Not connected
10	Not connected	9	Not connected
12	Not connected	11	GND
14	GND	13	C0p- Upstream2
16	C0p- Downstream2	15	C0n- Upstream2
18	C0n- Downstream2	17	GND
20	GND	19	Not connected
22	Not connected	21	Not connected
24	Not connected	23	GND

Table 24: X1 (2) unidirectional links

Pin #	Signal name	Pin #	Signal name
2	GND	1	C0p- DirectionA
4	Not connected	3	C0n- DirectionA
6	Not connected	5	GND
8	GND	7	Not connected
10	Not connected	9	Not connected
12	Not connected	11	GND
14	GND	13	C0p- DirectionB
16	Not connected	15	C0n- DirectionB
18	Not connected	17	GND
20	GND	19	Not connected
22	Not connected	21	Not connected
24	Not connected	23	GND

Rearranging Wires in the Probe Connector

If your design is not consistent with the previous link configuration recommendations, you must disassemble and rewire the connectors at the module end of the probe.

The wires can be rearranged in any way as long as you observe the following guidelines:

- x16 links require two modules, and each side of the link must have all of the lanes grouped together on the module end connectors (upstream with upstream and downstream with downstream).
- The mid-bus footprint can have multiple links on it, but the module end connectors must only have a uni-directional link on it or a bi-directional link less than x16.

A bi-directional module can handle a single link of x8, x4, x2, or x1 with no routing restrictions to the module end connectors.

If you have questions or concerns about reordering the wires in the probe, please contact a Tektronix support representative.

NOTE. *You can only rearrange wires in the connector at the module end of the probe, not in the probe head.*

1. Press gently on either side of the connector to snap off the cover. You will see that each of the wires is labeled. Identify the wire you want to remove from the connector.

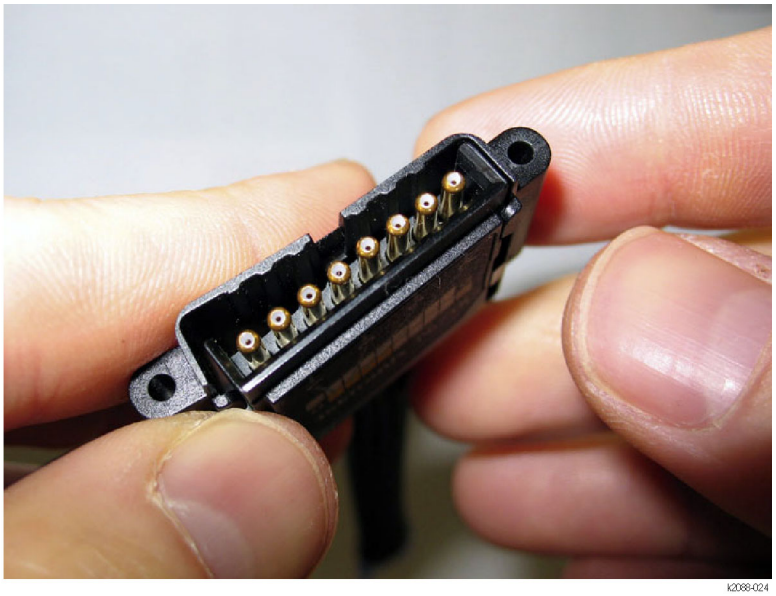


Figure 44: Opening the probe connector

2. Remove the probe sleeve anchor from the connector, and pull the sleeve away from the connector so that the wire labels are exposed.

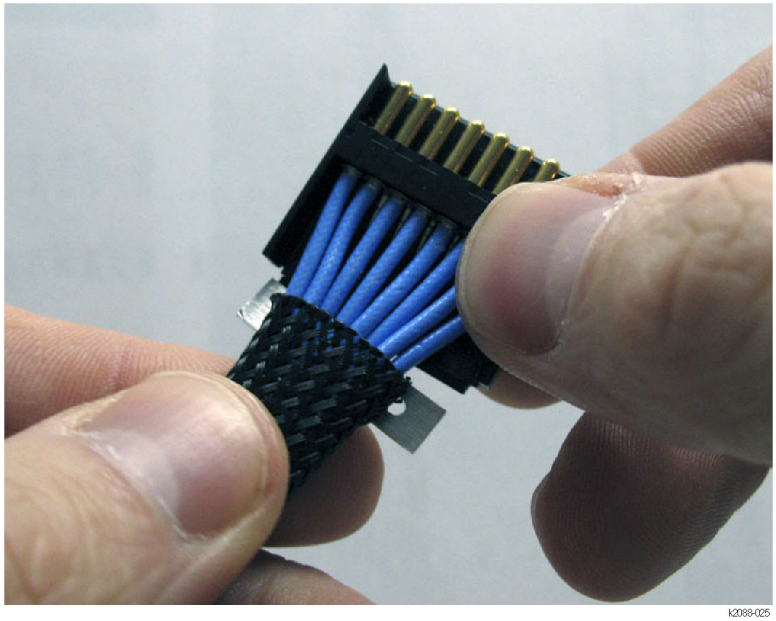


Figure 45: Removing the probe sleeve

3. Use the labels on the wires to determine the new order for the wires in the connector.

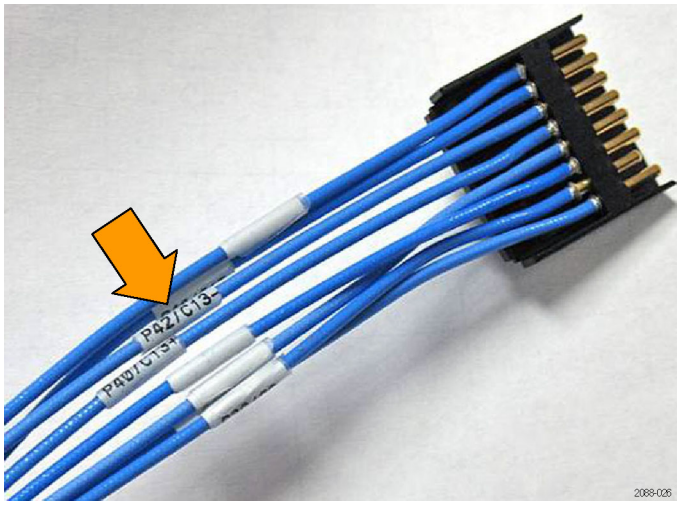


Figure 46: Probe labels

4. Use a bent paper clip (or similar tool) to press downward on the plastic retainer in the connector until the wire slides out. Repeat for the second wire.

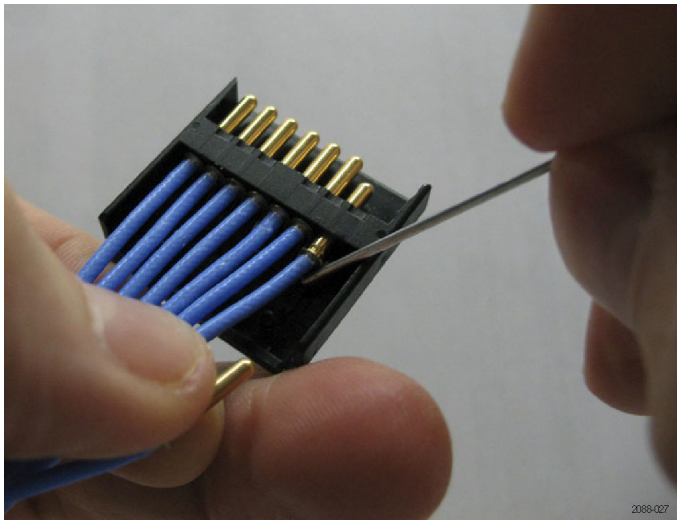


Figure 47: Removing individual wires

5. Repeat step 3 for the wire that you want to put in its place.
6. Insert the replacement wire, making sure the plastic retainer holds it securely. You will feel and hear the connector snap in place.
7. Replace the probe sleeve and the connector cover.

Adding Probes to the P6701SD Probe Connector

The P6701SD probe ships with two signal wires (one differential pair) in the 8-pin signal connector that connects to the serial analyzer module. The 8-pin connector can accommodate up to three additional probes, for a total of four probes per connector.

To add, remove, or rearrange probes in the connector, refer to the illustrations in the previous section and perform the following procedure. (See page 54, *Rearranging Wires in the Probe Connector*.)

1. Press gently on either side of the connector to snap off the cover.
2. Remove the probe sleeve anchor from the connector, and pull the sleeve away from the connector.
3. Use a bent paper clip (or similar tool) to press downward on the plastic retainer in the connector until the cable slides out. Repeat for the second cable.
4. Insert the wires from the additional probe into the connector, making sure the plastic retainer holds it securely. You will feel and hear the connector snap in place.

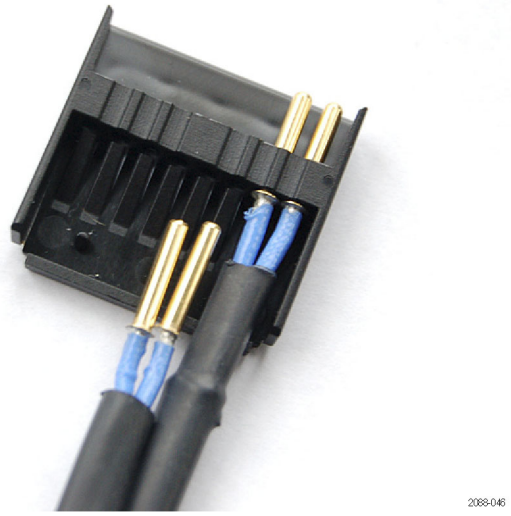


Figure 48: Inserting additional probe wires

5. Repeat step 4 for additional probes as needed.
6. Replace the probe sleeve and the connector cover.

Specifications

Environmental

The following table lists atmospheric specifications for the P67xx Series probes. The Operating specifications apply when the probe is connected between a compatible serial analyzer module and a system under test.

Table 25: Atmospheric characteristics

Characteristic		Description
Temperature	Operating	+0 °C to +50 °C
	Nonoperating	-40 °C to +74 °C
Humidity	Operating	5% to 95% relative humidity up to +30 °C
		5% to 75% relative humidity up to +50 °C
	Nonoperating	5% to 95% relative humidity up to +30 °C
		5% to 75% relative humidity up to +60 °C
Altitude	Operating	3000 m (9843 ft)
	Nonoperating	12,192 m (40,000 ft)

For a complete list of specifications including overall system specifications, refer to the *TLA7S08 & TLA7S16 Product Specification & Performance Verification Technical Reference Manual* (Tektronix part number 071-2270-xx). The manual is available on the TLA Family Documentation Browser CD (Tektronix part number 063-3671-07 or higher), or you can download the files from the Tektronix Web site.

Maintenance

The P67xx Series Serial Analyzer Probes do not require scheduled maintenance. However, the P6701SD solder-down probe contains replaceable bullet contacts in the probe head. Instructions for replacing the contacts are described below. To verify basic functionality of the probes, refer to the *TLA7S08 & TLA7S16 Serial Analyzer Modules Instruction Manual*.

Bullet Contacts

The input sockets in the probe body assembly are protected by preinstalled, replaceable bullet contacts. The bullet contacts protect the input sockets by absorbing the wear from repeated connect/disconnect cycles of the accessory tips. The bullet contacts are rated for 100 connect/disconnect cycles. Exceeding this number may degrade the performance of the probe.

An optional bullet tool is used to replace the bullet contacts from the probe body assembly. A kit of four replacement bullets is available as an optional accessory for the probe. See the *P6701SD Solder-Down Logic Analyzer Probe Installation Manual* for replacement part numbers.

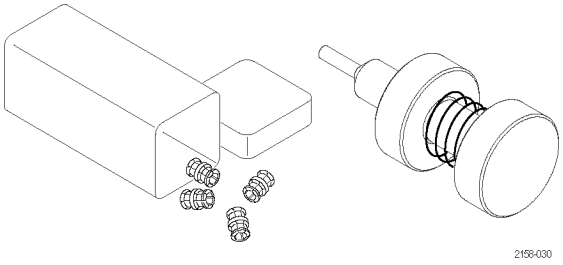


Figure 49: Replaceable bullets and tool

CAUTION. *To prevent wear to the probe housing, use only the bullet tool to remove and install the bullets from the probe body assembly. To prevent damage to the probe, before you connect accessories to the probe body, always check that the contacts are located in the probe body only.*

Removing the Bullets

Follow these steps to remove the bullets by using the removal tool:

1. Squeeze the tool plunger to extend the holder tangs.
2. Insert the tool into the probe body so that the holder tangs surround one of the bullets.

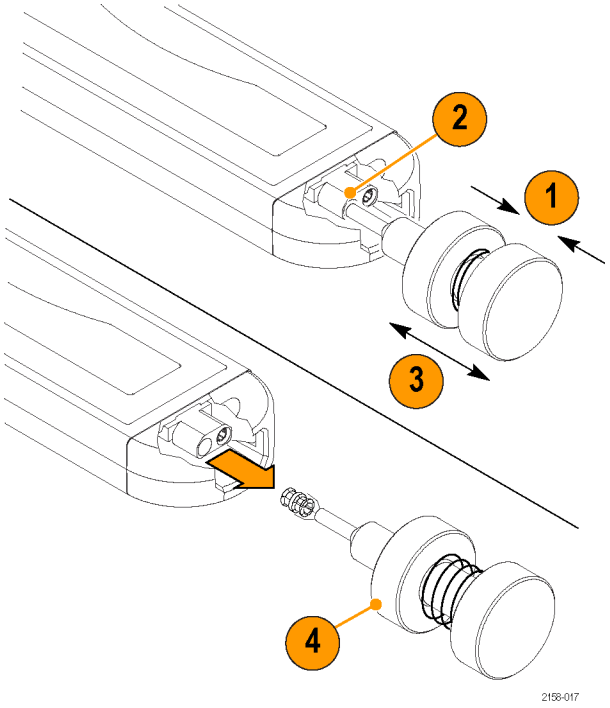


Figure 50: Removing the bullet contacts

3. Release the plunger to secure the holder tangs on the bullet.
4. Gently pull the tool outward to remove the bullet.
5. Repeat for the other bullet.

Inspecting the Bullets and Connectors

Use a microscope to closely examine the bullets and connectors. Use the illustrations to determine if the contacts appear worn or broken, and always replace them in pairs.

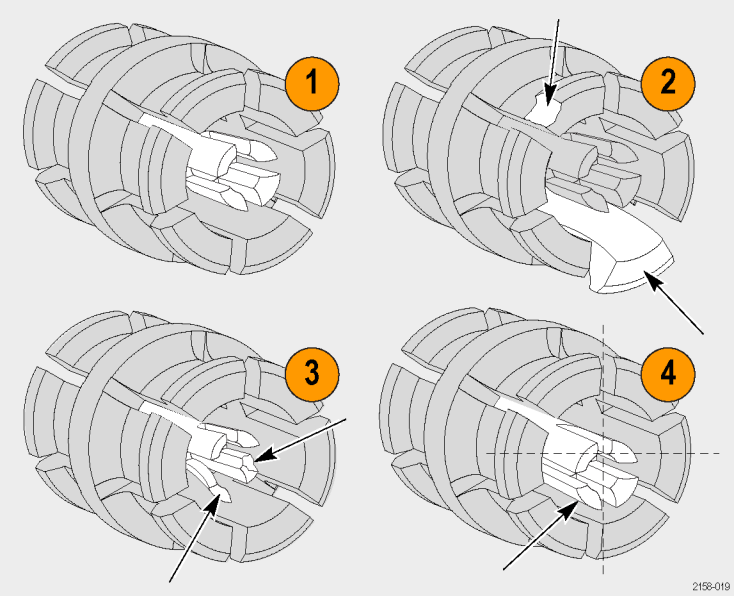


Figure 51: Inspect the bullet contacts

1. Good
2. Chipped or bent ground contacts (outer conductor)
3. Chipped or bent signal contacts (inner conductor)
4. Inner contacts misaligned to outer conductor

Installing the Bullets

1. Squeeze the tool plunger to extend the holder tangs.
2. Insert a new bullet into the tool so that the holder tangs surround the bullet.
3. Release the plunger to secure the holder tangs on the bullet.
4. Insert the tool into the probe body and seat the bullet in the recess.

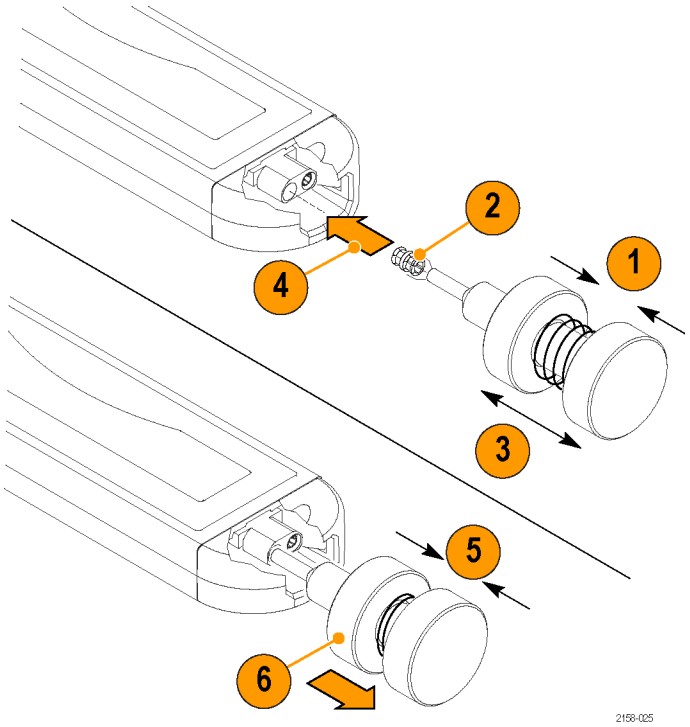


Figure 52: Installing the bullet contacts

5. Squeeze the tool plunger to release the bullet.
6. Gently pull the tool out of the probe body.
7. Repeat for the other bullet.
8. Test that the bullets are installed correctly by connecting and then removing the solder tip to the probe head. Inspect the probe head and verify that the bullets remain seated in the probe head.

Inspection and Cleaning

Keep the probes free of dirt, dust, and contaminants to maintain a reliable electrical probe connection.

Cleaning the Retention Mechanism

If the retention mechanism appears to be dirty, clean it as follows:

CAUTION. *To avoid electrical damage, always power off your system under test before cleaning the retention mechanism.*

1. Remove any lint using a nitrogen air gun or clean, oil-free dry air.

Cleaning the Probe Head

Remove any lint using a nitrogen air gun or clean, oil-free dry air. Avoid brushing or rubbing the contacts. Never use abrasive cleaners or organic solvents.

Storing the Probe

When not in use, store the probe in the Tektronix-supplied transport case.

Repackaging Instructions

Use the original packaging, if possible, to return or store the probe. If the original packaging is not available, use a corrugated cardboard shipping carton. Add cushioning material to prevent the probe from moving inside the shipping container.

Enclose the following information when shipping the probe to a Tektronix Service Center.

- Owner's address
- Name and phone number of a contact person
- Type of probe
- Reason for return
- Full description of the service required

Appendix A: PCI Express System Design Review Checklist

Use the following tables as a guide to review your system design.

General Considerations

Your system design must allow you to physically connect a mid-bus, slot interposer, or solder-down probe to each of the PCI Express links in the system. If this seems impossible, contact your local Tektronix representative for an alternative solution.

Mid-bus Probe Configuration

Table 26: Mid-bus Probe Configuration

Pass	Fail	N/A	Description
☐	☐	☐	Each mid-bus footprint is configured according to one of the pin-channel assignment formats recommended in this manual. [1]
☐	☐	☐	A reference clock cable connector (if required) is provided for each PCI Express reference clock domain. [2]
☐	☐	☐	All reference clocks are properly terminated in the system.

1 If your design requires you to use a pin-channel assignment that is not recommended, please contact your local Tektronix representative for help.

2 A reference clock connector is required if SSC (spread spectrum clocking) is enabled or can not be disabled. A reference clock connector is also required if the link frequency is intentionally margin tested outside the standard +/-150 ppm tolerance, or the link reference operates outside the +/-150 ppm tolerance imposed by the current tools.

Mechanical Considerations

Table 27: Mid-bus Probe

Pass	Fail	N/A	Description
☐	☐	☐	Each mid-bus footprint is designed according to the specifications provided in this document, including:
☐	☐	☐	Pad size, spacing, arrangement
☐	☐	☐	Hole sizes, locations, tolerance, plating
☐	☐	☐	Solder mask requirements
☐	☐	☐	Pad plating requirements

Table 27: Mid-bus Probe (cont.)

Pass	Fail	N/A	Description
☐	☐	☐	Pin numbering
☐	☐	☐	Footprint keep-out requirements
☐	☐	☐	Probe keep-out requirements
☐	☐	☐	Egress for probe cables is provided.

Table 28: Slot Interposer Probe

Pass	Fail	N/A	Description
☐	☐	☐	System design provides the physical space needed for the probe and the PCI Express add-in card that plugs into the probe, including:
☐	☐	☐	Probe keep-out requirements
☐	☐	☐	Egress for probe cables is provided.
☐	☐	☐	Any special requirements (cables, add-ons) for the PCI Express card have been met.
☐	☐	☐	The thermal requirements of the PCI Express card have been met. (The card will be out of its normal position when the interposer probe is installed.)
☐	☐	☐	If a reference clock is provided on the PCI Express card, verify that it meets the reference clock probe keep-out requirements while connected to the probe.

Table 29: Reference Clock Connector

Pass	Fail	N/A	Description
☐	☐	☐	Each reference clock connector matches the specifications in this manual, including:
☐	☐	☐	Verify that the dimensions are equivalent to the suggested part specification for either the SMT connector (Samtec FTR-103-02-S-S) or the through-hole connector (Samtec TMS-103-02-S-S). Check pad and hole size, spacing, arrangement, etc.
☐	☐	☐	Verify pin assignment (Pin 1 = REFCLKp or REFCLKn, Pin 2 =GND, Pin3 = REFCLKn or REFCLKp.)

Table 29: Reference Clock Connector (cont.)

Pass	Fail	N/A	Description
☐	☐	☐	Verify that adequate space exists on the board. Review the reference clock keep-out requirements in this manual.
☐	☐	☐	Verify that egress for reference clock cables is provided.

Electrical Considerations

Table 30: Mid-bus Probe

Pass	Fail	N/A	Description
☐	☐	☐	System loss and jitter due to the footprint has been calculated and the values meet the requirements for the P6716 and P6708 serial analyzer modules.
☐	☐	☐	The requirements for AC coupling capacitor location have been met. (Each pair of capacitors may be placed on either side of the mid-bus footprint for each differential signal pair, but the location relationship can be varied for different differential pairs in the link.)
☐	☐	☐	For each link probed, system simulations have been performed with load models included in order to verify that the system will work with mid-bus probes attached. Verify that the loss and jitter at the system receivers is within specifications when the probe load is present.
☐	☐	☐	For each link probed using a mid-bus footprint, system simulations have been performed with the footprint load model included in order to verify that the system will work with the footprint *without* the probe attached
☐	☐	☐	The system layout follows the guidelines in this manual, including:
☐	☐	☐	Via and trace requirements
☐	☐	☐	Differential pair routing (matched length, identical paths/vias, etc.)
☐	☐	☐	Pin-channel assignment of each mid-bus footprint matches a suggested format provided in this manual:
☐	☐	☐	All channels of a single direction of a link connect to the same footprint. It is preferable (but not required) that both directions of a link connect to the same footprint.

Table 31: Slot Interposer Probe

Pass	Fail	N/A	Description
☐	☐	☐	For each PCI Express slot that supports the use of an interposer, loss and jitter at the card connector has been calculated and the values meet the requirements for the P6716 and P6708 serial analyzer modules.
☐	☐	☐	For each PCI Express slot probed, system simulations have been performed with slot interposer probe load models included in order to verify that the system will work with a slot interposer probe connected.
☐	☐	☐	Loss and jitter at the system receivers is within spec when the slot interposer probe load is included.

Table 32: Reference Clock Connector

Pass	Fail	N/A	Description
☐	☐	☐	Reference clock electrical requirements have been met, including:
☐	☐	☐	Differential voltage requirements
☐	☐	☐	Absolute voltage requirements
☐	☐	☐	Frequency requirements
☐	☐	☐	Simulations of the reference clock network(s) have been performed using load models for the reference clock connector to ensure good signal integrity to the serial module.

Appendix B: Reference Files

S-parameter and load model data are included in the electronic files that are attached to the PDF file of this document. To view the files, open the PDF file and click on the Attachments tab on the lower-left side of the document. The following files are included:

- s-param DATs explained.txt
- sdd12wop.dat
- sdd12wp.dat
- P6701SD.dat

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